Jim Rodge

SERIAL REMOTE I/O BOARD

MODEL S-16

Son-Rich B

I/O CONTROLS INC.
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Newtown, Pennsylvania 18940
Phone (215) 860-8088

S-16 Notes

- Generates interrupt every 13.3 ms while key is down
- Need to wait for a delay of ~30 ms without character interrupt to know key is released — generated by timer B with timer C as a prescaler
- 38-8 allows 128 keys

~~STD129~~

~~4.9152 osc for timers~~

~~J11-8 to J12-7 Timer C out to Timer B in~~

Time Log Breakdown

DONKEY WALK

3/2/85	ANIMATE + INSERT	COMPILE	C.S.	P.B.	F.S.
Scene 1 KF1	35 MIN + = 35 MIN				
Scene 1 WC	138 MIN + 19 MIN =192 MIN	88 MIN	14 MIN	5 MIN	5 SEC
Scene 2	3 MIN + 3 MIN = 6 MIN	11 MIN		4 MIN	34 SEC
Scene 3	+ 9 MIN = 9 MIN	2 MIN			26 SEC
Scene 4 *	16 MIN + 26 MIN = 42 MIN	25 MIN	40 MIN	5 MIN	13 SEC
Fix Up **	11 MIN + 10 MIN = 21 MIN	17 MIN	9 MIN		
TOTAL	=305 MIN	143 MIN	63 MIN	14 MIN	78 SEC

WC= WALK CYCLE

* = Scene 4`s actual completion time took the same as Scene 3, however the reason for the extra time is because of a "File Space Exausted" message that occured due to unecessary data that was stored on the disk. Dave had to spend extra time in these modes to fix the problem.

**= Fix Up animation that needed to be adjusted because of changes on taping stratagies.

3/3/85	ANIMATE + INSERT	COMPILE	C.S.	P.B.	F.S.
GRISTMILL	177 MIN + 10 MIN =187 MIN	8 MIN	22 MIN	7 MIN	7 SEC
TOTAL	=187 MIN	8 MIN	22 MIN	7 MIN	7 SEC

3/4/85	ANIMATE + INSERT	COMPILE	C.S.	P.B.	F.S.
AHAB	30 MIN + 6 MIN = 36 MIN	7 MIN	9 MIN	11 MIN	4.2 SEC
TOTAL	= 36 MIN	7 MIN	9 MIN	11 MIN	4.2 SEC

S-16 Changes

— Power: None if no LED's + 7805 not too hot
describe how configured

— IRQ: ✓Remove R9 R8 and Q1

✓Connect U11-12 + 13 to U6-3 (~~R8~~)

✓Connect U11-11 to $\overline{IRQ}$ (~~Q1C~~ R9)

(Makes $\overline{IRQ}$ into RS232) (~~STD 129 J72 10-11, nonstandard, connective RS232 for I5 J12, 9, 10 + change to I4~~)

~~[illegible]~~

— Data out: ✓Remove D1

~~Short~~ D2

(Eliminates paralleling of data out)

~~— Board select: ✓Pull address select jumper common to +5 (4.7K to near end of R11) (board always selected)~~

— ✓Baud rate, clock rate: both to #1 (9600, 153.6 KHz clock)
Each scan line state is 831 µS with clock divisor = 2

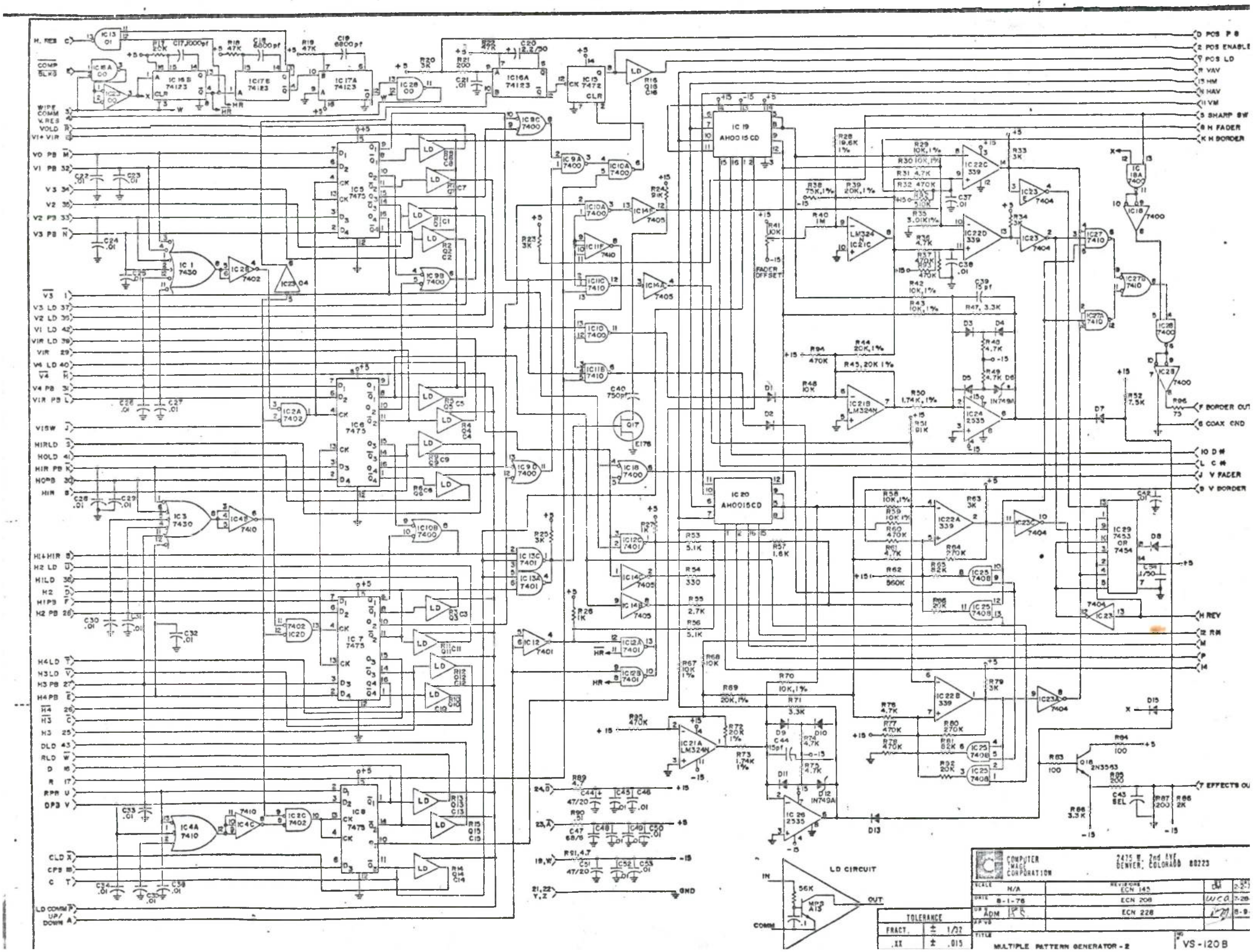
~~64 × 77 KHz scan rate~~

~~64 × 13 µS scan period~~

~~64 × .2 mS for ~~#~~ 16 ~~steps~~ (twice around 8 banks)~~

~~13.3 mS for 16 steps~~

— U16, 17, 18, 19 pins 3, 6, 9, 12 to gnd at U17-7
cut etch on component side from U18-6 toward U9
isolates drivers from $\overline{BD}$ signal of 8279, allows all switch columns to work



COMPUTER IMAGE CORPORATION
2475 W. 2nd AVE
DENVER, COLORADO 80223

SCALE N/A	REVISIONS ECN 145	DM	2-2-
DATE 8-1-76	ECN 208	wca	7-28
DR. ADM RS.	ECN 228		8-9-
APVD			

TITLE MULTIPLE PATTERN GENERATOR - 2

NO. VS-120B

TOLERANCE	
FRACT.	± 1/32
.XX	± .015

S 16 / 8279 Init

Board addr = 1 or tied hi
Baud rate = 1 9600
clock rate = 1

L = literal
C = composite (requires 2 bytes) C command, D Data

	0 0	L	Reset 8279 (HW) (delay reqd ?)
	0 1	L	Latch card addr 1 (or tie addr sel line high)
	1 1	L	
1 2 A 2	2 2	C C	set divisor
1 0 A 8	0 8	C C	Mode: 16 char, L entry, Encoded scan KB, 2 key lockout
1 A A 0	A 0	C C	No write inhibit or blanking
1 D A 3	D 3	C C	clear display (all 0) + FIFO
1 4 A 0	4 0	C C	set for read of FIFO

---

write CC - composite command - send in 2 bytes

#1 = 0001, command hi nibble

#2 = 1010, command lo nibble

---

write CD - composite data - 2 bytes

0001, data hi nibble

1000, data lo nibble

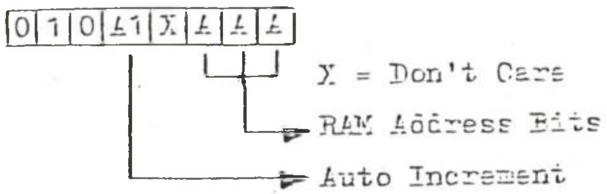
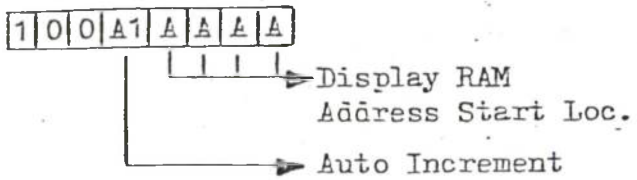
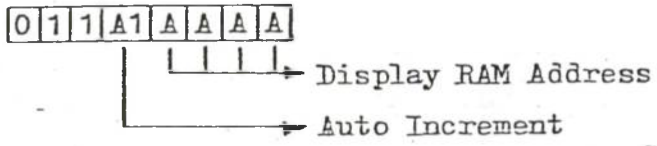
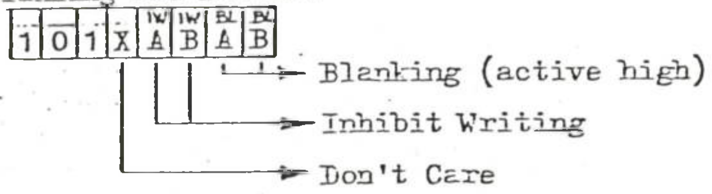
---

to read data: first set read display or read FIFO command NO - never in read display
then 0100 xxxx and wait for char to come back

to read status: send 0110 xxxx + wait for character in

---

to get incoming keystroke: Generate interrupt ~~from~~ if ever ~~read display RAM~~ NO S-16 $\overline{IRQ}$ line, then send read data command (Read FIFO 8279 command first?) (read status first?) + when RXD int comes, reading RXD is code of depressed key.

Description	Command Word	1st	2nd
Read FIFO/Sensor RAM  0 1 0 A1 X A A A X = Don't Care RAM Address Bits Auto Increment Example: Start read at 0 - Auto Increment toggle read line 8 times (once for each read)	50	20	B5
End Interrupt (Restores $\overline{IRQ}$ if set Required after reading sensor RAM)	E0	20	BE
Write Display RAM  1 0 0 A1 A A A A Display RAM Address Start Loc. Auto Increment Example: Start at 0 and Auto Increment 1001 0000 = 90 To write data 2X = Lower nibble data 9X = Upped nibble data + $\overline{WR}$	90 	20 2X	B9 9X
Read Display RAM  Example: Start at 0 and Auto Increment 0111 0000 - 70 Toggle read lines	70	20 40	B7
Blanking and Inhibit  1 0 1 X A B A B IW IW BL BL Blanking (active high) Inhibit Writing Don't Care Example: Blank Display 1 0 1 0 0 0 1 1 - A3 Restore Display 1 0 1 0 0 0 0 0 - A0	A3 A0	23 20	BA BA

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215 860 8088

John Vernon Sales
Dick Bowman Engr
Jim Rodgers Engr

SERIAL REMOTE I/O BOARD

MODEL S-16

Son - Rich Bowman

```
  #####################
 #######################
#########################
####
#### #####       ######
#### #####      ########
####  ###     #####    ###
####  ###    ####      ###
####  ###   ####       ###
#### ########## ########
#### #########   ######
####
#########################
 #######################
  #####################
```

I/O CONTROLS, Inc.
517 E. Lincoln Hwy.
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215-757-2772

S-16
SERIAL REMOTE I/O BOARD

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SERIAL REMOTE I/O BOARD

Model S-16

General Description:

The S-16 peripheral card is designed to provide remote display output and sensor or keyboard input. This data is communicated to and from a host computer via RS-232-C interface. There are provisions for up to fifteen (15) S-16 cards to be wired to one RS-232-C port on the host computer and to be individually addressed.

A UART is on board to convert serial data from the host to 8 bit parallel data for the S-16, and 8 bit parallel data to serial data for transmission to the host. Of the 8 bit word communicated to the S-16, the lower nibble is data and the upper nibble is used for control on the card. The serial data input is high impedance and the serial output is tri-state to allow for parallel operation of fifteen cards.

The S-16 is IC-14 (8279) which is the heart of programmable keyboard/display interface chip. It is software programmable for various operating modes including scanned keyboard, scan sensor matirx, strobed input entry, 2 key lockout, N key rollover, and 8 or 16 character display with right or left entry.

There are eight (8) keyboard or sensor input lines and four (4) scan lines. The scan lines can be programmed for encoded or decoded operation. In the encoded mode the 3 least significant scan lines can be decoded into 8 lines externally. This will allow use of a standard 64 key keyboard or 64 sensors (with external diode matrixing). Shift and control lines are available for keyboard operation.

Shift or control allows encoding 4 scan lines (8×16)

The scan lines are also used for the multiplexed display. They are decoded onboard and buffered and converted to open collector outputs capable of sinking 500 ma for convenient LED display driving.

The 8 display data lines are also buffered and converted so as to be able to provide 500 ma source at a user supplied voltage (card edge pins 55 and 56). how to control LED current - external series resistors

This 8 bit data output can be treated as a single 8 bit port for use with 7 segment displays or split into two 4 bit ports for use with hexadecimal displays. Using it as a split port can actually increase display capacity to 32.

Circuit Description:

Serial communication capability is provided by IC-1, General Instrument AY-3-1015D, UART chip. "Serial Data In", on card pin # 49 is a high impedance input to allow more than one card to share a single RS-232-C line. "Data Out", on card pin # 50 is a tri-state output again to allow multiple card use of a single RS-232-C line. Baud rate is jumper selectable from 150 to 9600 Baud.

Address decoding is accomplished by IC-3, (4514), 1 of 16 decoder and latch. The desired address is jumpered on the board. When all bits in

0000 aaaa } latch address
0001 aaaa
any but 0000 xxxx control/data bytes

the upper nibble are 0, the lower nibble functions as an address and the decoded address is latched when any bit in the upper nibble is toggled high. RD-4 is a logical choice for this toggled bit since it will not affect any other operation. The address will stay latched until 0 appears in the upper nibble again and a new address is latched. Care must be taken not to transmit a 0 in the upper nibble until another card is to be addressed.

After an address is latched the lower nibble becomes data until another card is to be addressed. Since we only have 4 bits of data available and 8 are needed, IC-12 and IC-13 act as tri-state latches. The latch on both devices is controlled by RD-4. When RD-4 is 0, RD-0 thru RD-3 become the data on DB-0 thru DB-3. When RD-4 is 1, RD-1 thru RD-3 become DB-4 thru DB-7. Data that was present when RD-4 was 0 is now held on the output of IC-12 as DB-o - DB-3.

When IC-1 receives data, DAV (pin 19) goes high and is presented to the data inputs of IC-2 which is a dual 4 bit static shift register. This bit is clocked thru by the Baud rate generator. IC-2B is always functional. Whenever data is transmitted by the host to any card on the line all IC-2Bs on the cards clock the DAV bit from IC-1 thru. On the first clock pulse after DAV, Q0 goes high and resets DAV thru pin 18 of IC-1, RDAV. After 3 more clock pulses Q3 goes high and enables a gate of IC-6 (pins 4,5, and 6). If the upper nibble is 0, a high condition will will be present at pin 5 and pin 6 and will enable IC-3 which will cause the lower nibble to be decoded as an address.

If this card's address was previously selected and is still latched, pins 9,10,11, and 12 of IC-7 will be high. The output pin 13 will be low and will allow DAV to clock thru IC-2A shift register also. At Q0 the data available at IC-12 or IC-13 (whichever is enabled by RD-4) will be clocked thru and emerge on the DB lines. At Q1 $\overline{WR}$ or $\overline{RD}$ will be brought low depending upon which one was enabled by the upper nibble control lines. $\overline{WR}$ will be low if RD-7 is high. $\overline{RD}$ will be low if RD-6 is high. Q2 and Q3 will simply prolong a read operation if RD-6 is high.

Control Bit Summary

write is 2 byte sequence out
Read is 1 byte out, 1 return

U/L

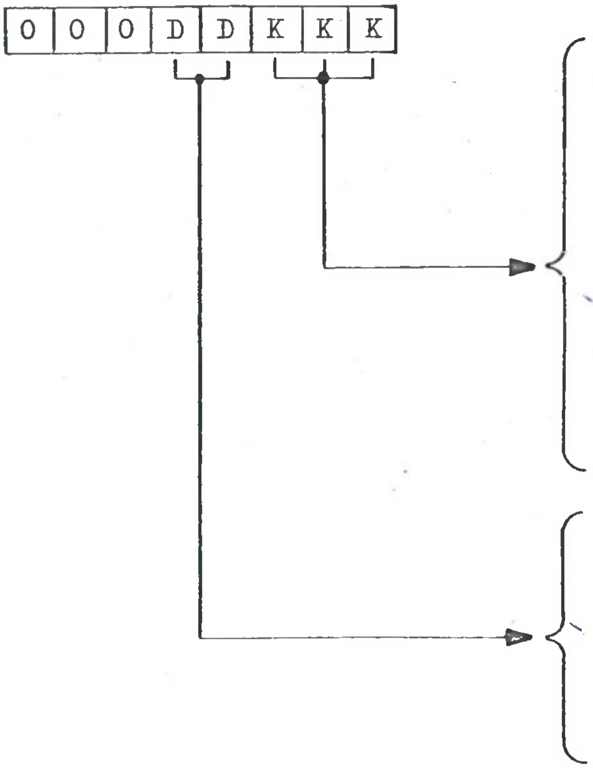
Bit 4	Data Nibble Select - 1=upper, 0=lower
Bit 5	$C\overline{D}$ - 1=command, 0=data
Bit 6	RD - Read (active high)
Bit 7	WR - Write (active high)

not necessary to toggle to repeat

4-7=0 => 0-3 = addr, then bring one of 4-7 hi to latch add
Write hi nibble first, then low with WR (and $C\overline{D}$ as needed)

Input/Display Mode Set-Up:

Mode Set-up word



Input Modes

0 0 0 Encoded Scan Keyboard-2 Key Lockout
0 0 1 Decoded Scan Keyboard-2 Key Lockout
0 1 0 Encoded Scan Keyboard-N Key Rollover
0 1 1 Decoded Scan Keyboard-N Key Rollever
1 0 0 Encoded Scan Sensor Matrix
1 0 1 Decoded Scan Matrix
1 1 0 Strobed input, Encoded Display Scan
1 1 1 Strobed input, Decoded Display Scan

Display Modes

0 0 8 8-bit character display-Left entry
0 1 16 8-bit character display-Left entry
1 0 8 8-bit character display-Right entry
1 1 16 8-bit character display-Right ent

All modes are explained in detail further in this manual. This section will deal primarily with the make up of the mode setup word and how to correctly communicate it to the S-16 card once it's been assembled.

After keyboard and display modes are decided upon look at the above table to assemble the complete mode set up word. For example, if the user desired an encoded scan sensor matrix and sixteen 8-bit character display with left entry, the mode set up word would be 0000 1100 (OC_{16}).

To communicate this to the S-16 it must be sent as the lower nibble of two 8-bit words with the upper nibble containing control information for the S-16.

The first word transmitted would be 2C. The data nibble C is the lower nibble of our mode set up word OC. The control nibble 2 tells the S-16 to use the data nibble as the lower nibble to IC-14 by enabling IC-12 and disabling IC-13 and that this will be a command word because C/$\overline{D}$ is high.

The second word transmitted would be BO. The data nibble 0 becomes the upper nibble to IC-14 because we changed the control nibble to B from 2. This toggles RD-4 which now disables IC-12 and enables IC-13. It leaves C/$\overline{D}$ high as before and now since our mode set up word has been completely reassembled and is ready to be written to IC-14, a control B will cause the WR bit (RD7) to go high.

See P.25, 8279 Data Sheet

SL 0-3 decoded + buffered

Input Modes:

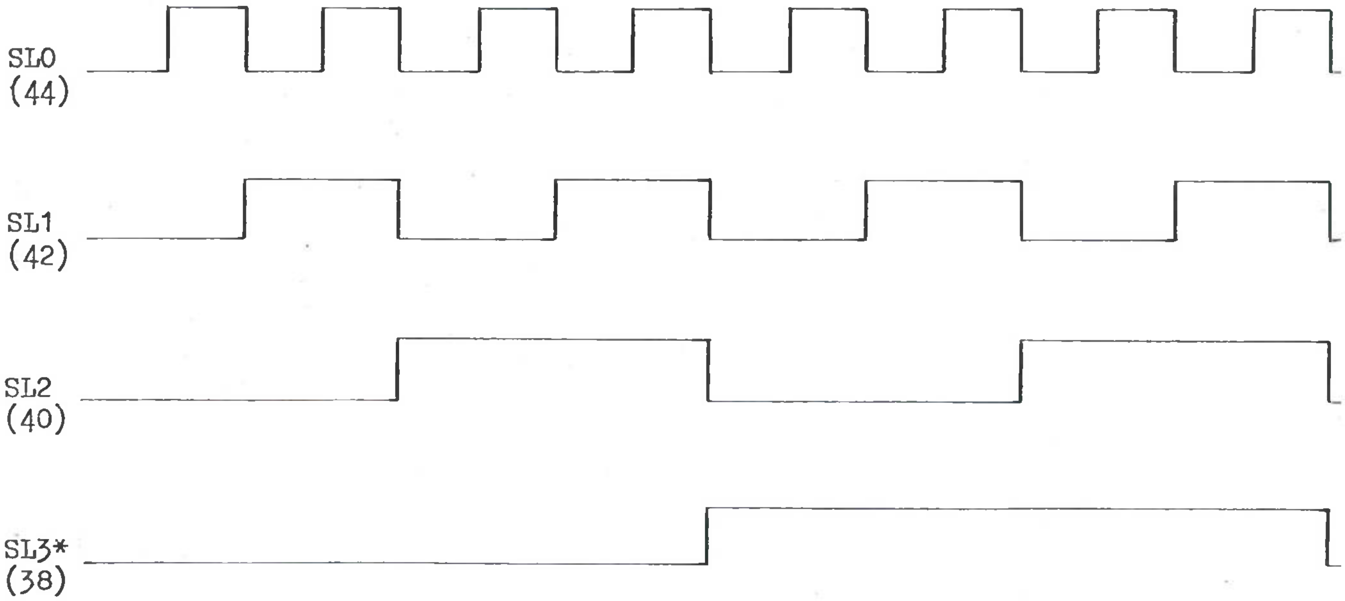
I. Scanned Keyboard

Scanned keyboard mode can be used with up to 64 key keyboards. There are 8 return lines available from the keyboard (card edge pins 37,39, 41,43,45,46,47, and 48). Four scan lines are provided (38,40,42 and 44). These scan lines can be programmed for either encoded scan (8 X 8 keyboard) or decoded scan (4 X 8 keyboard).

can use shift or Control inputs to scan 16 rows

In the encoded scan mode only the 3 LSB scan lines can be used. (SL-3 is used for display scanning only). These lines are brought to the card edge and must be decoded by the user with a 1 of 8 decoding device for this application. With the above mentioned 8 return lines the user is now provided with 8 rows of 8 bit of information allowing use of a 64 key keyboard. Encoded scan pulses are active high.

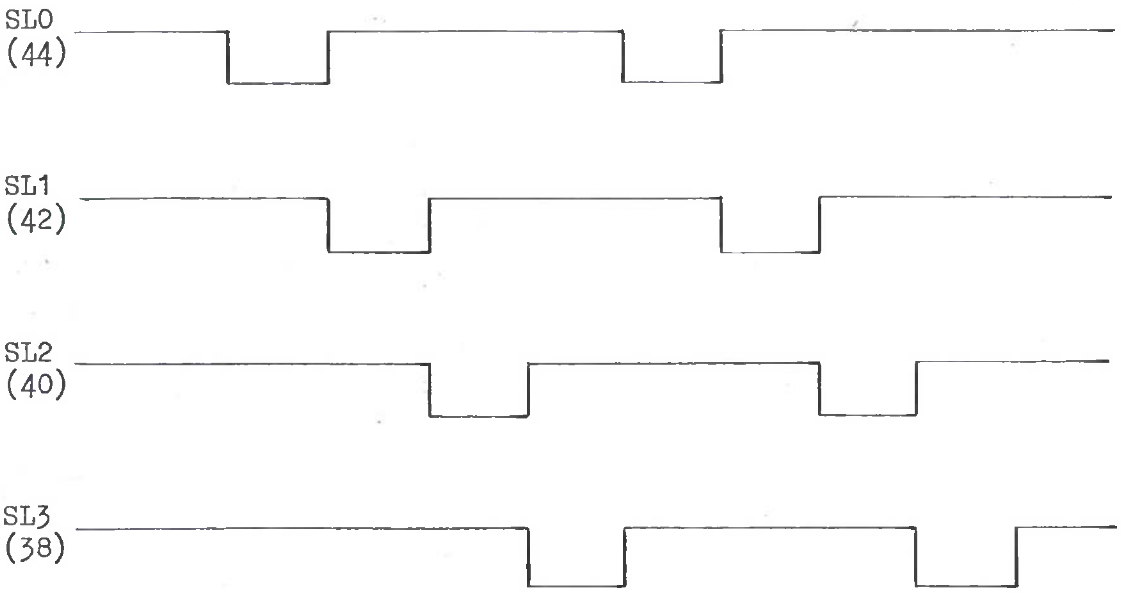
decoder on board



* Use only for display (not keyboard) in this mode.

unless connected to shift or Control

Decoded scan mode causes SL-0 → SL-3 to sequentially go low for 1 clock pulse each, eliminating the need for user decoding but limiting the number of rows which can be scanned to 4. This gives the user a 4 row by 8 bit configuration allowing use of a 32 key keyboard. Decoded scan pulses are active low. All 4 scan lines can be utilized in decoded scan mode.



An important point to consider in deciding whether to use encoded or decoded scan (besides the size of the keyboard) is the fact that the scan lines are shared by both the input and display section. This means that when using decoded scan mode for a 4 X 8 key keyboard only 4 displays will be usable.

In either scanning mode a key depression generates a 6 bit encoding of key position. Position and shift (pin 8) and control (pin 7) are stored in the FIFO. Keys are automatically debounced with 2 key lockout or N-key rollover which is software selectable.

II. Scanned Sensor Matrix Mode

This mode allows the user to substitute inputs other than keyboard keys into the system. If the possibility exists for more than one input to be active any any instant, which is an extremely likely possibility, the user must provide external diode isolation.

Debounce logic is inhibited in scanned sensor matrix mode. The status of the sensor is inputted directly to the sensor RAM. The sensor RAM becomes an image register reflecting the status of the switches in the sensor matrix.

The $\overline{\text{IRQ}}$ line goes low in this mode when any change in the sensor RAM is detected. The board must be addressed for $\overline{\text{IRQ}}$ to be gated to the edge connector (pin 10). If only one board is being used it can be left addressed after system initialization. If more than one board is on a single RS-232-C line the host must interrogate each board to check for an $\overline{\text{IRQ}}$ signal. This relieves the host of having to constantly look at the entire sensor RAM and check for changes on all cards. The $\overline{\text{IRQ}}$ line is cleared by the first data read operation if the Auto-Increment flag is set to zero, or by the End Interrupt command if Auto-Increment is set to one.

III. Strobed Input Mode

The control line (pin 7) becomes a strobe input in this mode. It has an internal pull up. When pulled low it causes data on return lines to be transferred to FIFO.

IV. Display Modes:

Eight or sixteen 8-bit character modes with right or left entry can be programmed into IC-14. 8-bit characters allow use of 7-segment displays with decimal point (segments A → G and DP).

When using left entry mode each display position directly corresponds to a byte in the Display RAM. RAM address 0 is the left - most display character and address 15 (or address 7 in 8 character display) is the right - most display character. Entering characters from position zero causes the display to fill from the left. The 17th (9th) character is entered back in the left - most position etc.

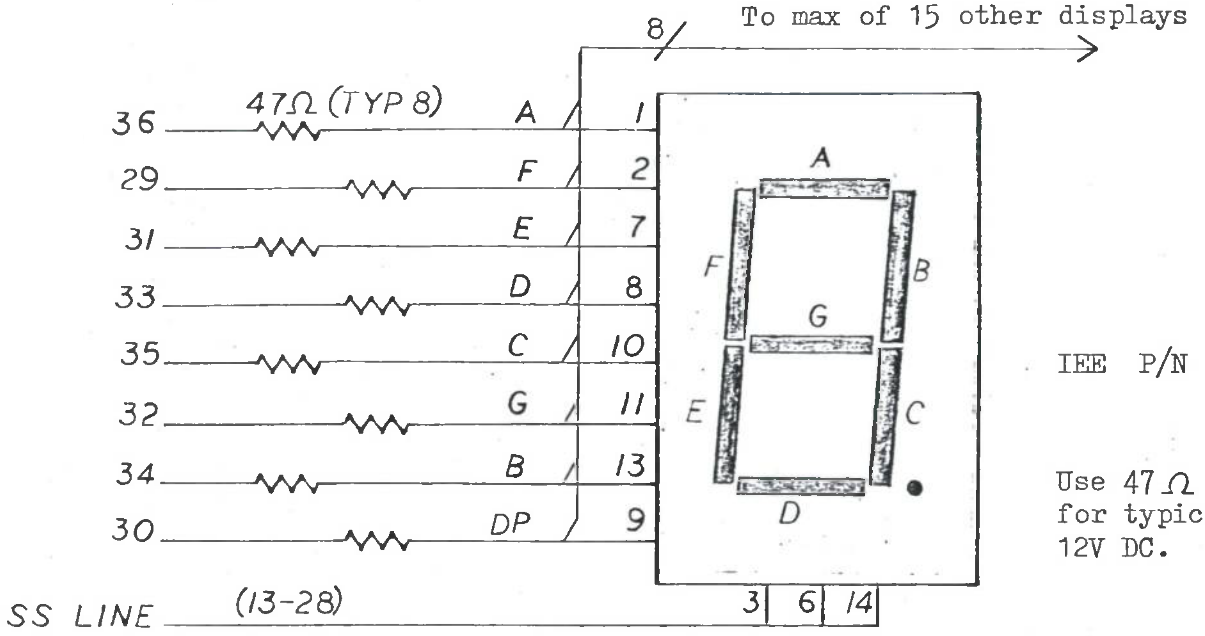
When using right hand entry the first and all entries are placed in the right - most display character. Each time a new entry is given all previous entries shift one to the left. The left - most entry shifts off the display and is lost.

Display Use and Control:

The Display RAM is organized as sixteen 8-bit words using only 8 bytes for an 8 character display and all 16 bytes for a 16 character display. Information in the Display RAM is automatically scanned to the card edge 8 bits at a time on pins 29 thru 36. The voltage sourced to these pins depends on the voltage the user applies to pins 55 and 56. Maximum ratings are 15V at 500 ma. These 2 pins can be jumpered on board to +5 volts for low power uses. Most display applications will require an external voltage source to provide the necessary voltage and current needed to drive 7-segment LED displays.

The common pin of the user's 7-segment displays is connected to the appropriate scan line on pins 13 thru 28. These scan select lines are active low open collector outputs capable of sinking 500 ma. per output.

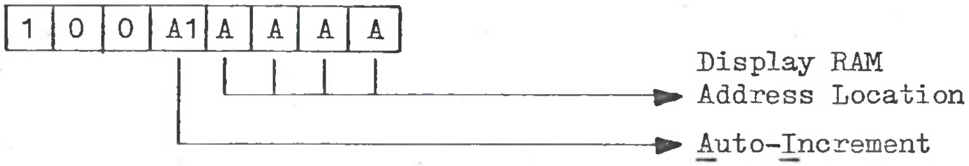
Typical connections are shown below:



IEE P/N 1723R

Use 47Ω resistors for typical supply of 12V DC.

The host must first set up the S-16 with the following command word to write to Display RAM:



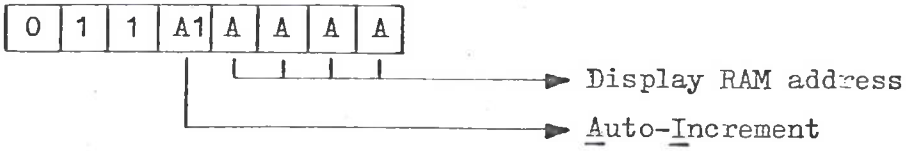
To communicate this command to the S-16 the host must break it into upper and lower nibble which are each used as the lower nibble of the 8 bit work transmitted to the S-16. The upper nibble will consist of control bits.

For Example: To write 16 characters in sequence to the Display RAM using the Auto-Increment function and beginning at RAM address 0, the command word would be 90. The first word to the S-16 would be 20. The data nibble 0 is the lower nibble of the command word. The control nibble 2, tells the S-16 to use the transmitted 0 as the lower nibble by enabling IC-12 and disabling IC-13 (RD4=0). The second word transmitted to the S-16 will be B9. The data nibble 9 will be used by the S-16 as the upper nibble data because the control word B will cause RD-4 to toggle high reversing the enable states on IC-12 and IC-13. It will also cause IC-14 to accept the now fully assembled command word 90 on lines DB0 thru DB7.

Now that IC-14 is set up to write to Display RAM we must communicate data to it. Again, two words must be transmitted serially to communicate one data word. 2X will communicate the lower nibble. 9X will communicate the upper nibble and command the write. This sequence can then be completed 16 times to communicate data to all 16 displays.

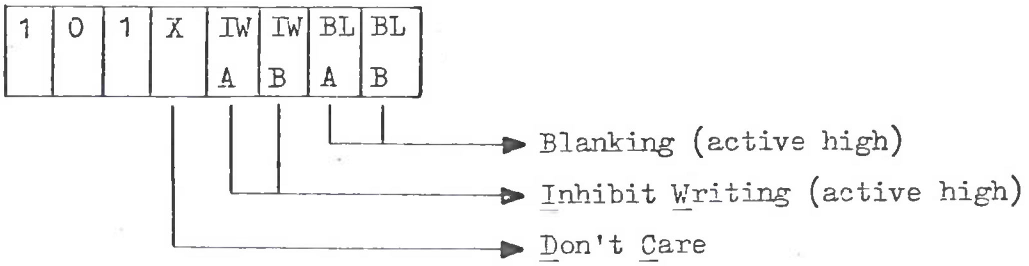
Once data is in the Display RAM it will be continuously scanned to the display. Any single or combination of displays can be changed by writing new data to the Display RAM address specifically.

The host can access display RAM either as a single location or in an Auto-Increment mode where the read line is toggled to step through Display RAM from the address in the Read Display Command Word:



The previously outlined procedure for transmitting data to the S-16 in two 8 bit word fashion must be followed.

The host also has the ability to inhibit writing to the Display RAM and also to blank the display. The following command word incorporates both these functions:



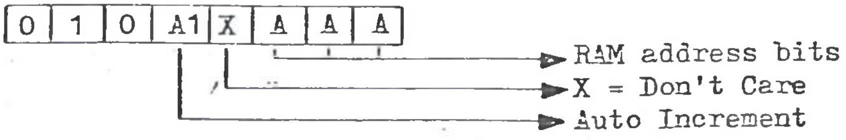
Since it is possible to use the output as 2 4-bit ports instead of 1 8-bit as assumed in all previous discussions IW and BL functions are set up so that either lower (A) or upped (B) nibbles can be operated upon separately.

FIFO/Sensor RAM:

FIFO/Sensor is a dual function 8 X 8 RAM. It is FIFO RAM in keyboard or strobed input modes. Each new entry is written into successive RAM locations and when a read operation is commanded, information is read in order of entry. An $\overline{IRQ}$ signal is given when FIFO is not empty.

This block becomes Sensor RAM in scanned sensor matrix mode with each row of RAM indicating the status of the corresponding row of sensors in the sensor matrix. In this mode an $\overline{IRQ}$ signal is given when a change in sensor RAM is detected.

The host sets up the S-16 for a FIFO/Sensor RAM read by first writing this command:



In scan keyboard mode Auto Increment and RAM address bits are irrelevant. The data bus of IC-14 will be driven each subsequent read [$\overline{\text{CD}}$ (RD5) = 0] in the same sequence in which the data first entered FIFO by toggling the $\overline{\text{RD}}$ line (RD-6). Until another command is transmitted to the S-16 all subsequent reads will be from FIFO.

In the sensor matrix mode one of 8 rows of sensor RAM is chosen by the RAM address bits (AAA). If the Auto Increment bit is high each toggle of the read line will cause the next row of sensor RAM to be read.

Remember, only 4 bits of data can be transmitted to the S-16 card at a time. So to transmit the above command word 4 bits of data and 4 bits of control will be transmitted twice; lower nibble, then upper nibble.

Example: In scanned sensor matrix mode the host receives an $\overline{\text{IRQ}}$ signal and wants to interrogate sensor RAM to determine which sensor has changed state. The command word to start at RAM address 0 and automatically step through RAM by toggling the RD line is 0101 0000 or 50_{16}.

Assuming this S-16 card has already been addressed we would want to transmit the lower nibble first by sending 20 to the S-16. By sending the upper nibble 2 as a control word to the S-16 we are telling IC-14 not to do anything because we are keeping $\overline{\text{CD}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ lines all high.

The next word to the S-16 will be B5. The data word (lower nibble) 5 will become the upper nibble data to IC-14. The control word (upper nibble) B will cause the following to happen:

RD4 - High - Causing the data word 5 to appear on DB4 thru DB7

RD5 - High - Tells IC-14 this is a command word

RD6 - Low - Tells IC-14 this is not a road operation

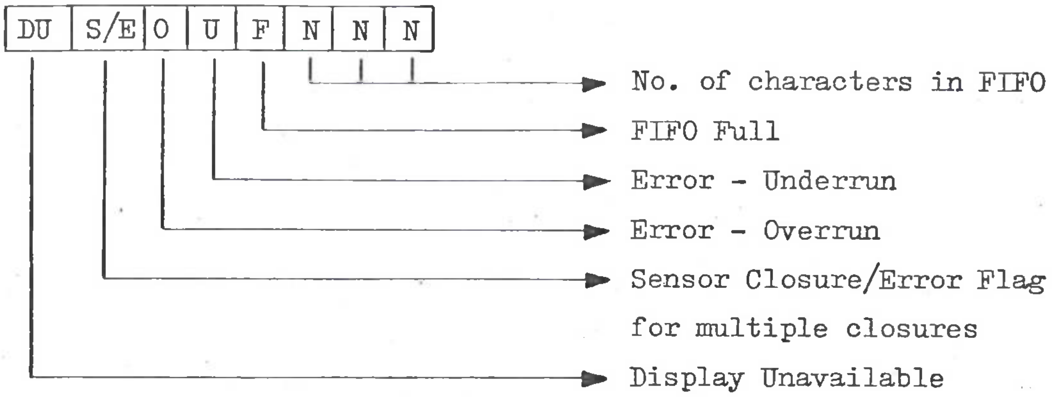
RD7 - High - Tells IC-14 this is a write operation

Now we have told IC-14 that we want to read sensor RAM starting at address 0. To actually get it to send this information back to us we must toggle the $\overline{\text{RD}}$ line of IC-14 by sending 40 8 times.

toggle 40-0-40 not necessary to repeat

Data from the S-16 is in full 8 bit bytes.

FIFO Status:



DU
S/E
O
U
F
N
N
N
No. of characters in FIFO
FIFO Full
Error - Underrun
Error - Overrun
Sensor Closure/Error Flag for multiple closures
Display Unavailable

The status word can be obtained by a read operation with ~~$\overline{\text{RD}}$~~ $C/\overline{D}$ high. This would require the word 6X to be communicated to the S-16. The lower nibble can be anything because IC-12 and IC-13 will be in a tri-state condition.

In scanned keyboard and strobed input modes FIFO status is used to indicate the number of characters in FIFO and whether an error has occurred. Overrun and underrun are the only two possible errors. Overrun occurs when the entry of another character into full FIFO is attempted. Underrun occurs when the host tries to read an empty FIFO.

Scanned sensor matrix mode uses FIFO status word to indicate that one or more sensor closures are contained in sensor RAM (S/E).

If Display RAM is unavailable due to an as of yet uncompleted clear display or clear all operation the Du bit will be high.

In special error mode simultaneous multiple closure is shown by the error flag which occurs in the S/E bit. (N Key Rollover only)

Scan Rate Programming:

Use clk = U8 pin 7 (9600 baud, 153,600 Hz) and divisor = 2 for 77 KHz clock, fastest available?

All timing and scanning signals for IC-14 are generated by the clock frequency presented to pin 3 after being divided by a programmable interger divisor. By programming a divisor of 2 with an input clock frequency of a scan rate of approximately 200 KHZ will be generated.

The divisor set up word is formatted as follows:

0	0	1	D	D	D	D	D

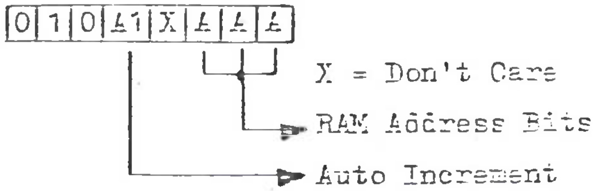
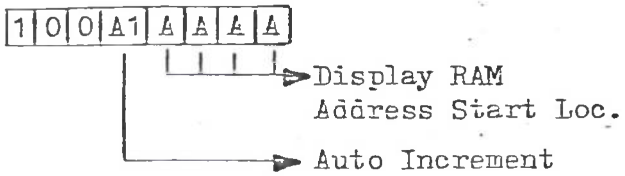
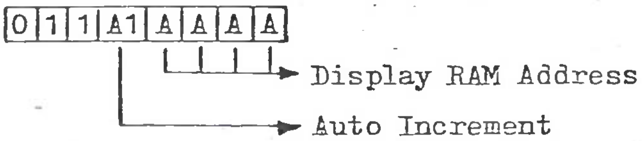
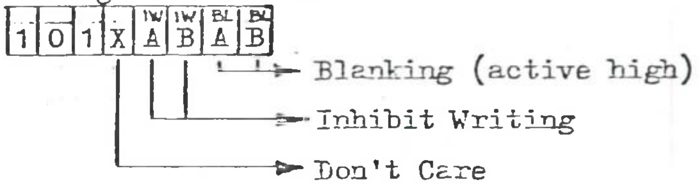
Binary value of divisor 2-31

A divisor of 2 would create a set up word of 22. This must be transmitted to the S-16 as two words which would be 22 and B2 respectively.

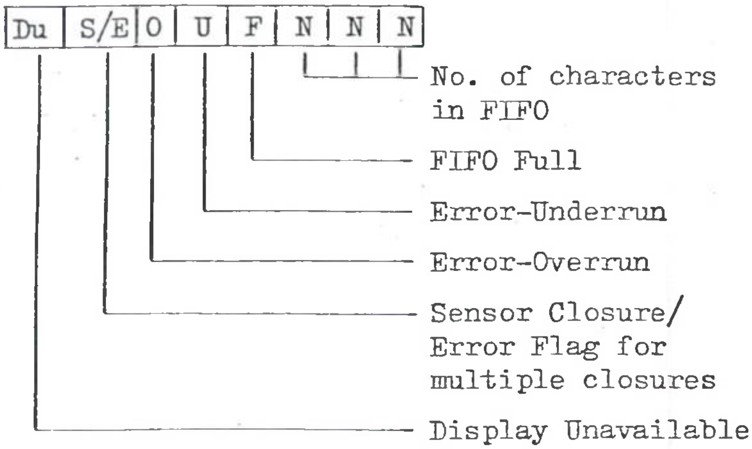
8279 (IC-14) Command Instructions:

To S-16

Description	Command Word	1st	2nd
Reset - Reset address decoder and latch IC-3 Resets all RAM functions on 8279 Places 8279 in following modes a) 16 8-bit character display -left entry b) Encoded scan keyboard -2 key lockout	00	00	
Addressing -(Where X is the jumpered address of the desired card	0X	0X	
Program Clock Divisor | 0 | 0 | 1 | D | D | D | D | D | (Where D is divisor in binary 2-31) Example → ÷ 2	22	22	B2
Mode Set Up Wrod | 0 | 0 | 0 | D | D | K | K | K | KKK 0 0 0 Encoded Scan Keyboard -2 key lockout 0 0 1 Decoded Scan Keyboard -2 key lockout 0 1 0 Encoded Scan Keyboard -N-key rollever 0 1 1 Decoded Scan Keyboard -N-key rollever 1 0 0 Encoded Scan Sensor Matrix 1 0 1 Decoded Scan Sensor Matrix 1 1 0 Strobed Input, Encoded Display Scan 1 1 1 Strobed Input, Decoded Display Scan DD 0 0 8 8-bit character display -left entry 0 1 16 8-bit character display -left entry 1 0 8 8-bit character display -right entry 1 1 16 8-bit character display -right entry Example: 16 8-bit display - left entry encoded scan sensor matrix 00001100 = 0C	0C	2C	B0

Description	Command word	1st	2nd
Read FIFO/Sensor RAM  0 1 0 A1 X A A A X = Don't Care RAM Address Bits Auto Increment Example: Start read at 0 - Auto Increment toggle read line 8 times (once for each read)	50	20	B5
End Interrupt (Restores $\overline{IRQ}$ if set Required after reading sensor RAM)	E0	20	BE
Write Display RAM  1 0 0 A1 A A A A Display RAM Address Start Loc. Auto Increment Example: Start at 0 and Auto Increment 1001 0000 = 90 To write data 2X = Lower nibble data 9X = Upped nibble data + $\overline{WR}$	90 	20 2X	B9 9X
Read Display RAM  Example: Start at 0 and Auto Increment 0111 0000 - 70 Toggle read lines	70	20 40	B7
Blanking and Inhibit  1 0 1 X IW A IW B BL A BL B Blanking (active high) Inhibit Writing Don't Care Example: Blank Display 1 0 1 0 0 0 1 1 - A3 Restore Display 1 0 1 0 0 0 0 0 - A0	A3 A0	23 20	BA BA

To S-16

Description	Command Word	1st	2nd
Read FIFO Status The following status word can be obtained by a read operation with $\overline{\text{CD}}$ high X = Don't Care  Du S/E O U F N N N No. of characters in FIFO FIFO Full Error-Underrun Error-Overrun Sensor Closure/ Error Flag for multiple closures Display Unavailable	6X	6X	

GENERAL INSTRUMENT

AY-5-1013A AY-3-1014A
AY-6-1013 AY-3-1015D

GENERAL INFORMATION

UAR/T: Universal Asynchronous Receiver/Transmitter

FEATURES

- DTL and TTL compatible—no interfacing circuits required—drives one TTL load
- Fully Double Buffered—eliminates need for system synchronization, facilitates high-speed operation
- Full Duplex Operation—can handle multiple bauds (receiving-transmitting) simultaneously
- Start Bit Verification—decreases error rate with center sampling
- Receiver center sampling of serial input; 46% distortion immunity
- High Speed Operation
- Three-State Outputs—bus structure capability
- Low Power—minimum power requirements
- Input Protected—eliminates handling problems

AY-5-1013A

- GIANT P-channel nitride process
- 0 to 40kbaud
- Pull up resistors to V_{CC} on all inputs

AY-6-1013

- GIANT P-channel nitride process
- 0 to 22.5kbaud
- Extended Operating Temperature Range:
  -40°C to +85°C (plastic package)
  -55°C to +125°C (ceramic package)
- Pull-up resistors to V_{CC} on all inputs

AY-3-1014A/1015D

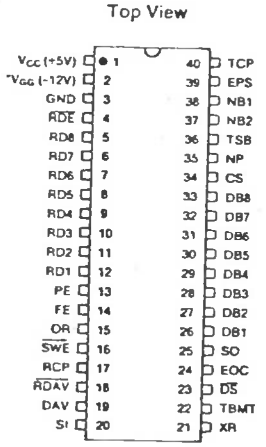
- Single Supply Operation:
  +4.75V to +14V (AY-3-1014A)
  +4.75V to +5.25V (AY-3-1015D)
- CMOS compatible (AY-3-1014A)
- 1½ stop bit mode
- External reset of all registers except control bits register
- GIANT II N-channel Ion Implant Process
- 0 to 30k baud
- Pull-up resistors to V_{CC} on all inputs (AY-3-1015D)

DESCRIPTION

The Universal Asynchronous Receiver/Transmitter (UAR/T) is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, one or two stop bits (1½ stop bit capability with the AY-3-1014A/1015D), and either odd/even parity or no parity. In order to make the UAR/T universal, the baud, bits per word, parity mode, and the number of stop bits are externally selectable. The device is constructed on a single monolithic chip. All inputs and outputs are directly compatible with MTOS/MTNS logic, and also with TTL/DTL/CMOS logic without the need for interfacing components. All strobed outputs are three-state logic.

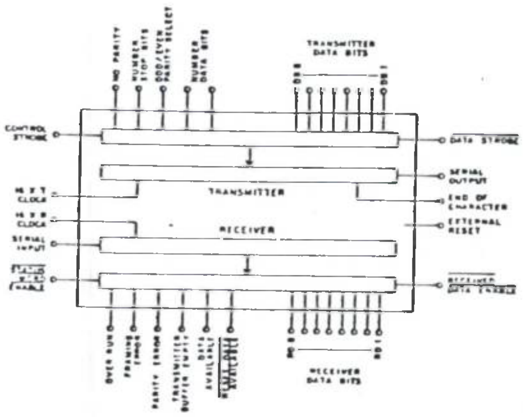
PIN CONFIGURATION

40 LEAD DUAL IN LINE



* Pin 2: AY-3-1014A/1015D — No Connection.

BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name (Symbol)	Function
1	V_{CC} Power Supply (V_{CC})	+5V Supply
2	V_{GG} Power Supply (V_{GG})	−12V Supply (Not connected for AY-3- 1014A/1015)
3	Ground (V_{GND})	Ground
4	$\overline{\text{Received Data Enable}}$ ($\overline{RDE}$)	A logic "0" on the receiver enable line places the received data onto the output lines.
5-12	Received Data Bits (RD8-RD1)	These are the 8 data output lines. Received characters are right justified: the LSB always appears on RD1. These lines have tri-state outputs; i.e., they have the normal TTL ouput characteristics when $\overline{RDE}$ is "0" and a high impedance state when $\overline{RDE}$ is "1". Thus, the data output lines can be bus structure oriented.
13	Parity Error (PE)	This line goes to a logic "1" if the received character parity does not agree with the selected parity. Tri-state.
14	Framing Error (FE)	This line goes to a logic "1" if the received character has no valid stop bit. Tri-state.
15	Over-Run (OR)	This line goes to a logic "1" if the previously received character is not read (DAV line not reset) before the present character is transferred to the receiver holding register. Tri-state.
16	$\overline{\text{Status Word Enable}}$ ($\overline{SWE}$)	A logic "0" on this line places the status word bits (PE, FE, OR, DAV, TBMT) onto the output lines. Tri-state.
17	Receiver Clock (RCP)	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud.
18	$\overline{\text{Reset Data Available}}$ ($\overline{RDAV}$)	A logic "0" will reset the DAV line. The DAV F/F is only thing that is reset. Must be tied to logic "1" when not in use on the AY-3-1014A.
19	Data Available (DAV)	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register. Tri-state. Fig. 12,34.
20	Serial Input (SI)	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception. Fig. 11,12,33,34.
21	External Reset (XR)	Resets all registers except the control bits register (the received data register is not reset in the AY-5-1013A and AY-6-1013). Sets SO, EOC, and TBMT to a logic "1". Resets DAV, and error flags to "0". Clears input data buffer. Must be tied to logic "0" when not in use.
22	Transmitter Buffer Empty (TBMT)	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character. Tri-state. See Fig. 18,20,40,42.
23	$\overline{\text{Data Strobe}}$ ($\overline{DS}$)	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of $\overline{DS}$. Data must be stable during entire strobe.
24	End of Character (EOC)	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character. See Fig. 17,19,39,41.
25	Serial Output (SO)	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted. See Fig. 16.
26-33	Data Bit Inputs (DB1-DB8)	There are up to 8 data bit input lines available.
34	Control Strobe (CS)	A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level.
35	No Parity (NP)	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "0".
36	Number of Stop Bits (TSB)	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits. For the AY-3-1014A/1015, the combined selection of 2 stop bits and 5 bits/character will produce 1½ stop bits.
37-38	Number of Bits/Character (NB2, NB1)	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits/character. NB2 NB1 Bits/Character 0 0 5 0 1 6 1 0 7 1 1 8
39	Odd/Even Parity Select (EPS)	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock (TCP)	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud.

TRANSMITTER OPERATION

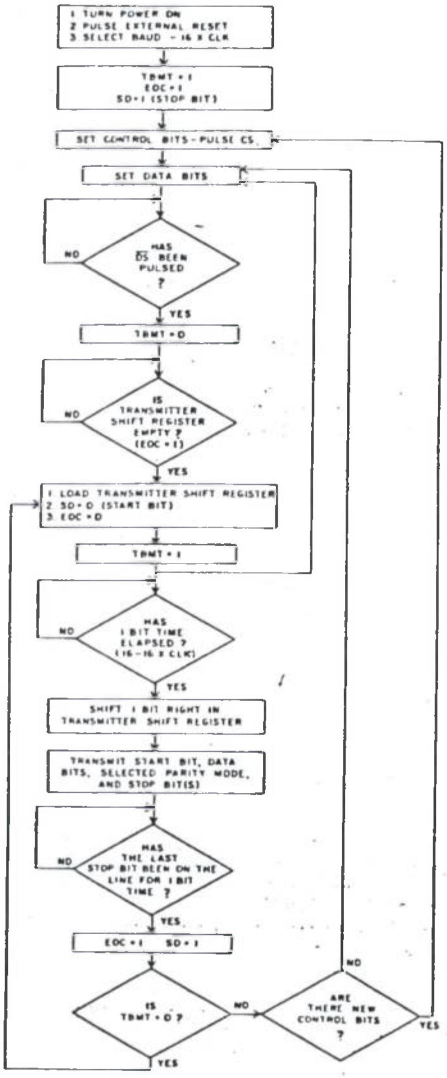

1 TURN POWER ON
2 PULSE EXTERNAL RESET
3 SELECT BAUD - 16 X CLK
TBMT = 1
EOC = 1
SO = 1 (STOP BIT)
SET CONTROL BITS - PULSE CS
SET DATA BITS
HAS DS BEEN PULSED ?
NO
YES
TBMT = 0
IS TRANSMITTER SHIFT REGISTER EMPTY ? (EOC = 1)
NO
YES
1 LOAD TRANSMITTER SHIFT REGISTER
2 SO = 0 (START BIT)
3 EOC = 0
TBMT = 1
HAS 1 BIT TIME ELAPSED ? (16 - 16 X CLK)
NO
YES
SHIFT 1 BIT RIGHT IN TRANSMITTER SHIFT REGISTER
TRANSMIT START BIT, DATA BITS, SELECTED PARITY MODE, AND STOP BIT(S)
HAS THE LAST STOP BIT BEEN ON THE LINE FOR 1 BIT TIME ?
NO
YES
EOC = 1 SO = 1
IS TBMT = 0 ?
NO
YES
ARE THERE NEW CONTROL BITS ?
NO
YES

Fig.1

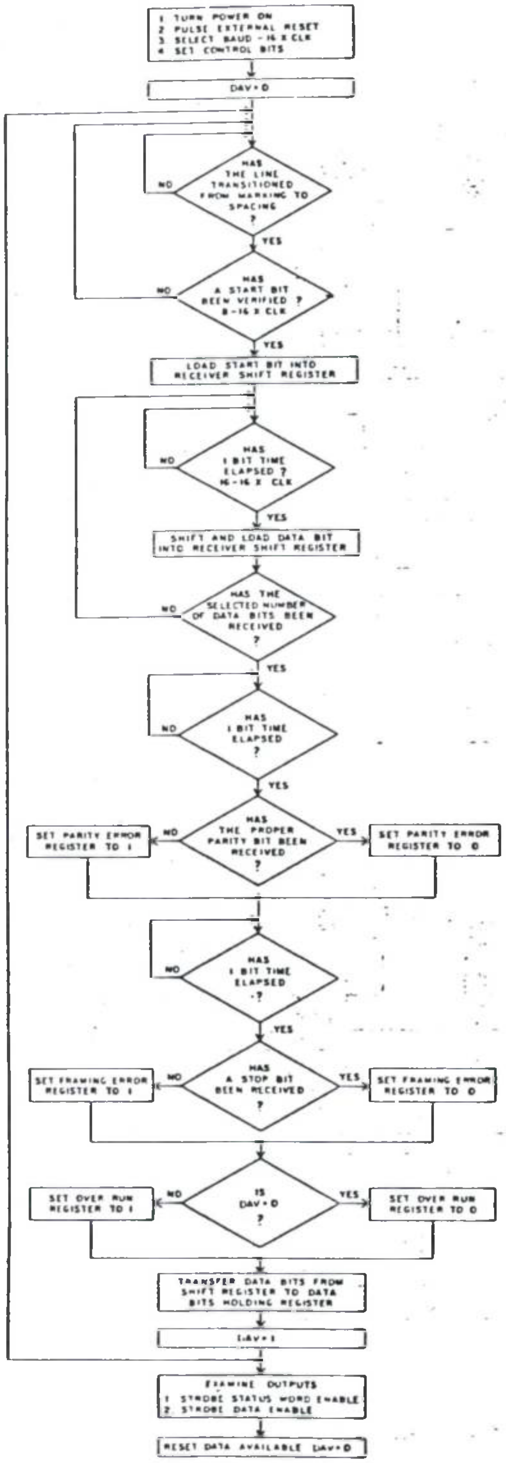
Initializing

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud. The above conditions will set TBMT, EOC, and SO to logic "1" (line is marking).

After initializing is completed, user may set control bits and data bits with control bits selection normally occurring before data bits selection. However, one may set both $\overline{DS}$ and CS simultaneously if minimum pulse width specifications are followed. Once Data Strobe ($\overline{DS}$) is pulsed the TBMT signal will change from a logic "1" to a logic "0" indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits, and transmitter shift register is transmitting previously loaded data. TBMT will return to a logic "1". When transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and EOC going to a logic "0", and TBMT will also go to a logic "1" indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering (separate data bits holding register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, EOC will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TBMT is a logic "0" as was previously discussed.

RECEIVER OPERATION



1 TURN POWER ON
2 PULSE EXTERNAL RESET
3 SELECT BAUD - 16 X CLK
4 SET CONTROL BITS
DAV = 0
HAS THE LINE TRANSITIONED FROM MARKING TO SPACING ?
NO
YES
HAS A START BIT BEEN VERIFIED ? 8 - 16 X CLK
NO
YES
LOAD START BIT INTO RECEIVER SHIFT REGISTER
HAS 1 BIT TIME ELAPSED ? 16 - 16 X CLK
NO
YES
SHIFT AND LOAD DATA BIT INTO RECEIVER SHIFT REGISTER
HAS THE SELECTED NUMBER OF DATA BITS BEEN RECEIVED ?
NO
YES
HAS 1 BIT TIME ELAPSED ?
NO
YES
SET PARITY ERROR REGISTER TO 1
NO
HAS THE PROPER PARITY BIT BEEN RECEIVED ?
YES
SET PARITY ERROR REGISTER TO 0
HAS 1 BIT TIME ELAPSED ?
NO
YES
SET FRAMING ERROR REGISTER TO 1
NO
HAS A STOP BIT BEEN RECEIVED ?
YES
SET FRAMING ERROR REGISTER TO 0
SET OVER RUN REGISTER TO 1
NO
IS DAV = 0 ?
YES
SET OVER RUN REGISTER TO 0
TRANSFER DATA BITS FROM SHIFT REGISTER TO DATA BITS HOLDING REGISTER
DAV = 1
EXAMINE OUTPUTS
1 STROBE STATUS WORD ENABLE
2 STROBE DATA ENABLE
RESET DATA AVAILABLE DAV = 0

Fig.2

Initializing

Power is applied, external reset is enabled, and clock pulse is applied having a frequency of 16 times the desired baud. The previous conditions will set data available (DAV) to a logic "1".

After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. Data reception starts when serial input signal changes from Marking (logic "1") to spacing (logic "0") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "0", the SI line continues to be at logic "0", when center sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs, the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (marking to spacing) when the 16x clock is in a logic "1" state, the bit time, for center sampling will begin when the clock line transitions from a logic "1" to a logic "0" state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip flop and/or the framing error flip flop to a logic "1". It should be noted that if the No Parity Mode is selected the PE (parity error) will be unconditionally set to a logic "0".

Once a full character is received, internal logic looks at the data available (DAV) signal to determine if data has been the read out. If the DAV signal is at a logic "1" the receiver will assume data has not been read out and the over run flip flop of the status word holding register will be set to a logic "1". If the DAV signal is at a logic "0" the receiver will assume that data has been read out. After DAV goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.

intel

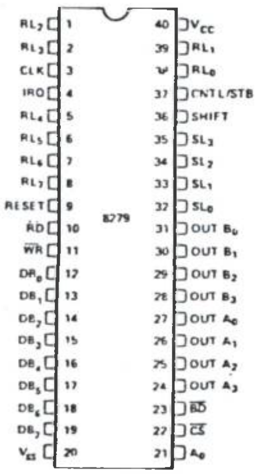
8279/8279-5
PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

- MCS-85™ Compatible 8279-5
- Simultaneous Keyboard Display Operations
- Scanned Keyboard Mode
- Scanned Sensor Mode
- Strobed Input Entry Mode
- 8-Character Keyboard FIFO
- 2-Key Lockout or N-Key Rollover with Contact Debounce
- Dual 8- or 16-Numerical Display
- Single 16-Character Display
- Right or Left Entry 16-Byte Display RAM
- Mode Programmable from CPU
- Programmable Scan Timing
- Interrupt Output on Key Entry

The Intel® 8279 is a general purpose programmable keyboard and display I/O interface device designed for use with Intel® microprocessors. The keyboard portion can provide a scanned interface to a 64-contact key matrix. The keyboard portion will also interface to an array of sensors or a strobed interface keyboard, such as the hall effect and ferrite variety. Key depressions can be 2-key lockout or N-key rollover. Keyboard entries are debounced and strobed in an 8-character FIFO. If more than 8 characters are entered, overrun status is set. Key entries set the interrupt output line to the CPU.

The display portion provides a scanned display interface for LED, incandescent, and other popular display technologies. Both numeric and alphanumeric segment displays may be used as well as simple indicators. The 8279 has 16X8 display RAM which can be organized into dual 16X4. The RAM can be loaded or interrogated by the CPU. Both right entry, calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto-increment of the display RAM address.

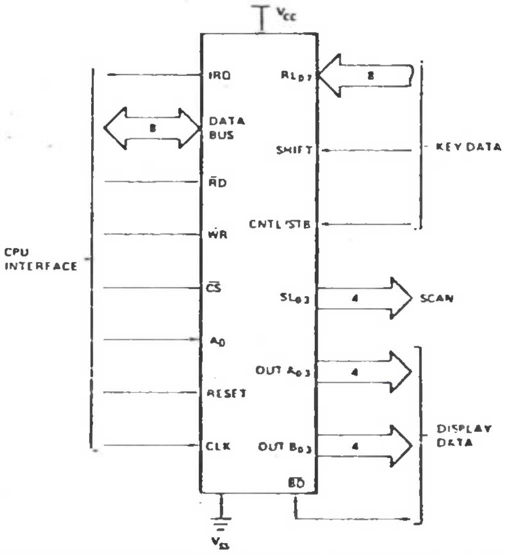
PIN CONFIGURATION



PIN NAMES

DB_{0-7}	I/O	DATA BUS (BI-DIRECTIONAL)
CLK	I	CLOCK INPUT
RESET	I	RESET INPUT
$\overline{CS}$	I	CHIP SELECT
$\overline{RD}$	I	READ INPUT
$\overline{WR}$	I	WRITE INPUT
A_0	I	BUFFER ADDRESS
IRQ	O	INTERRUPT REQUEST OUTPUT
SL_{0-3}	O	SCAN LINES
RL_{0-7}	I	RETURN LINES
SHIFT	I	SHIFT INPUT
CNTL/STB	I	CONTROL/STROBE INPUT
OUT A_{0-3}	O	DISPLAY (A) OUTPUTS
OUT B_{0-3}	O	DISPLAY (B) OUTPUTS
$\overline{BD}$	O	BLANK DISPLAY OUTPUT

LOGIC SYMBOL



HARDWARE DESCRIPTION

The 8279 is packaged in a 40 pin DIP. The following is a functional description of each pin.

No. Of Pins	Designation	Function
8	DB$_0$-DB$_7$	Bi-directional data bus. All data and commands between the CPU and the 8279 are transmitted on these lines.
1	CLK	Clock from system used to generate internal timing.
1	RESET	A high signal on this pin resets the 8279. After being reset the 8279 is placed in the following mode: 1) 16 8-bit character display —left entry. 2) Encoded scan keyboard—2 key lockout. Along with this the program clock prescaler is set to 31.
1	$\overline{CS}$	Chip Select. A low on this pin enables the interface functions to receive or transmit.
1	A$_0$	Buffer Address. A high on this line indicates the signals in or out are interpreted as a command or status. A low indicates that they are data.
2	$\overline{RD}$, $\overline{WR}$	Input/Output read and write. These signals enable the data buffers to either send data to the external bus or receive it from the external bus.
1	IRQ	Interrupt Request. In a keyboard mode, the interrupt line is high when there is data in the FIFO/Sensor RAM. The interrupt line goes low with each FIFO/Sensor RAM read and returns high if there is still information in the RAM. In a sensor mode, the interrupt line goes high whenever a change in a sensor is detected.
2	V$_{SS}$, V$_{CC}$	Ground and power supply pins.
4	SL$_0$-SL$_3$ outputs	Scan Lines which are used to scan the key switch or sensor matrix and the display digits. These lines can be either encoded (1 of 16) or decoded (1 of 4).
8	RL$_0$-RL$_7$	Return line inputs which are connected to the scan lines through the keys or sensor switches. They have active internal pullups to keep them high until a switch closure pulls one low. They also serve as an 8-bit input in the Strobed Input mode.
1	SHIFT	The shift input status is stored along with the key position on key closure in the Scanned Keyboard modes. It has an active internal pullup to keep it high until a switch closure pulls it low.
1	CNTL/STB	For keyboard modes this line is used as a control input and stored like status on a key closure. The line is also the strobe line that enters the data into the FIFO in the Strobed Input mode. (Rising Edge). It has an active internal pullup to keep it high until a switch closure pulls it low.
4 4	OUT A$_0$-OUT A$_3$ OUT B$_0$-OUT B$_3$	These two ports are the outputs for the 16 x 4 display refresh registers. The data from these outputs is synchronized to the scan lines (SL$_0$-SL$_3$) for multiplexed digit displays. The two 4 bit ports may be blanked independently. These two ports may also be considered as one 8 bit port.
1	$\overline{BD}$	Blank Display. This output is used to blank the display during digit switching or by a display blanking command.

~~). Of Pins Designation Function~~

Func Descr P.27

PRINCIPLES OF OPERATION

The following is a description of the major elements of the 8279 Programmable Keyboard/Display interface device. Refer to the block diagram in Figure 1.

I/O Control and Data Buffers

The I/O control section uses the $\overline{CS}$, A$_0$, $\overline{RD}$ and $\overline{WR}$ lines to control data flow to and from the various internal registers and buffers. All data flow to and from the 8279 is enabled by $\overline{CS}$. The character of the information, given or desired, by the CPU, is identified by A$_0$. A logic one means the information is a command or status. A logic zero means the information is data. $\overline{RD}$ and $\overline{WR}$ determine the direction of data flow through the Data Buffers. The Data Buffers are bi-directional buffers that connect the internal bus to the external bus. When the chip is not selected ($\overline{CS}$ = 1), the devices are in a high impedance state. The drivers input during $\overline{WR} \bullet \overline{CS}$ and output during $\overline{RD} \bullet \overline{CS}$.

ØD

Control and Timing Registers and Timing Control

These registers store the keyboard and display modes and other operating conditions programmed by the CPU. The modes are programmed by presenting the proper command on the data lines with A$_0$ = 1 and then sending a $\overline{WR}$. The command is latched on the rising edge of $\overline{WR}$.

Go to P.28

FUNCTIONAL DESCRIPTION

Since data input and display are an integral part of many microprocessor designs, the system designer needs an interface that can control these functions without placing a large load on the CPU. The 8279 provides this function for 8-bit microprocessors.

The 8279 has two sections: keyboard and display. The keyboard section can interface to regular typewriter style keyboards or random toggle or thumb switches. The display section drives alphanumeric displays or a bank of indicator lights. Thus the CPU is relieved from scanning the keyboard or refreshing the display.

The 8279 is designed to directly connect to the microprocessor bus. The CPU can program all operating modes for the 8279. These modes include:

Input Modes

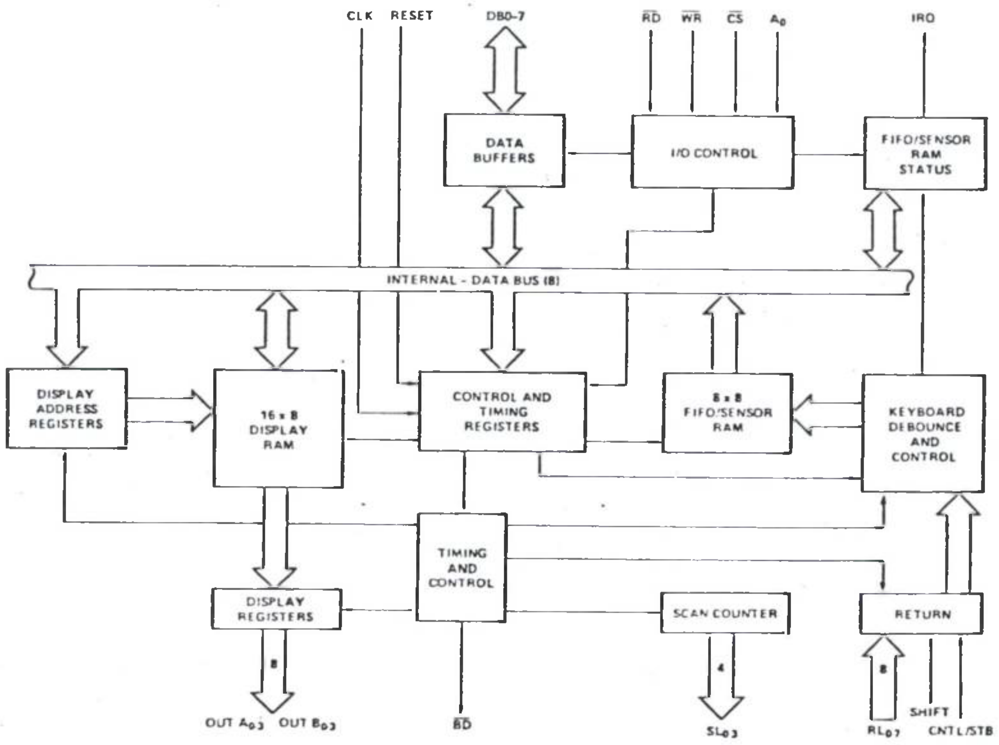
- Scanned Keyboard — with encoded (8 x 8 key keyboard) or decoded (4 x 8 key keyboard) scan lines. A key depression generates a 6-bit encoding of key position. Position and shift and control status are stored in the FIFO. Keys are automatically debounced with 2-key lockout or N-key rollover.
- Scanned Sensor Matrix — with encoded (8 x 8 matrix switches) or decoded (4 x 8 matrix switches) scan lines. Key status (open or closed) stored in RAM addressable by CPU.
- Strobed Input — Data on return lines during control line strobe is transferred to FIFO.

Output Modes

- 8 or 16 character multiplexed displays that can be organized as dual 4-bit or single 8-bit ($B_0 = D_0$, $A_3 = D_7$).
- Right entry or left entry display formats.

Other features of the 8279 include:

- Mode programming from the CPU.
- Clock Prescaler
- Interrupt output to signal CPU when there is keyboard or sensor data available.
- An 8 byte FIFO to store keyboard information.
- 16 byte internal Display RAM for display refresh. This RAM can also be read by the CPU.



00742A

from p. 26

The command is then decoded and the appropriate function is set. The timing control contains the basic timing counter chain. The first counter is a ÷ N prescaler that can be programmed to yield an internal frequency of 100 kHz which gives a 5.1 ms keyboard scan time and a 10.3 ms debounce time. The other counters divide down the basic internal frequency to provide the proper key scan, row scan, keyboard matrix scan, and display scan times.

Scan Counter

The scan counter has two modes. In the encoded mode, the counter provides a binary count that must be externally decoded to provide the scan lines for the keyboard and display. In the decoded mode, the scan counter decodes the least significant 2 bits and provides a decoded 1 of 4 scan. Note than when the keyboard is in decoded scan, so is the display. This means that only the first 4 characters in the Display RAM are displayed.

In the encoded mode, the scan lines are active high outputs. In the decoded mode, the scan lines are active low outputs.

(ie SC3 to Sh/ctrl works)

Return Buffers and Keyboard Debounce and Control

2 scans

The 8 return lines are buffered and latched by the Return Buffers. In the keyboard mode, these lines are scanned, looking for key closures in that row. If the debounce circuit detects a closed switch, it waits about 10 msec to check if the switch remains closed. If it does, the address of the switch in the matrix plus the status of SHIFT and CONTROL are transferred to the FIFO. In the scanned Sensor Matrix modes, the contents of the return lines is directly transferred to the corresponding row of the Sensor RAM (FIFO) each key scan time. In Strobed Input mode, the contents of the return lines are transferred to the FIFO on the rising edge of the CNTL/STB line pulse.

10.24 mS

FIFO/Sensor RAM and Status

This block is a dual function 8 x 8 RAM. In Keyboard or Strobed Input modes, it is a FIFO. Each new entry is written into successive RAM positions and each is then read in order of entry. FIFO status keeps track of the number of characters in the FIFO and whether it is full or empty. Too many reads or writes will be recognized as an error. The status can be read by an $\overline{RD}$ with $\overline{CS}$ low and A_0 high. The status logic also provides an IRQ signal when the FIFO is not empty. In Scanned Sensor Matrix mode, the memory is a Sensor RAM. Each row of the Sensor RAM is loaded with the status of the corresponding row of sensor in the sensor matrix. In this mode, IRQ is high if a change in a sensor is detected.

Display Address Registers and Display RAM

The Display Address Registers hold the address of the word currently being written or read by the CPU and the two 4-bit nibbles being displayed. The read/write addresses are programmed by CPU command. They also can be set to auto increment after each read or write. The Display RAM can be directly read by the CPU after the correct mode and address is set. The addresses for the A and B nibbles are automatically updated by the 8279 to match data entry by the CPU. The A and B nibbles can be entered independently or as one word, according to the mode that is set by the CPU. Data entry to the display can be set to either left or right entry. See Interface Considerations for details.

SOFTWARE OPERATION

8279 commands write

The following commands program the 8279 operating modes. The commands are sent on the Data Bus with $\overline{CS}$ low and A_0 high and are loaded to the 8279 on the rising edge of $\overline{WR}$.

C/$\overline{D}$

Keyboard/Display Mode Set

	MSB							LSB
Code:	0	0	0	D	D	K	K	K

Where DD is the Display Mode and KKK is the Keyboard Mode.

DD		
0	0	8 8-bit character display — Left entry
0	1	16 8-bit character display — Left entry*
1	0	8 8-bit character display — Right entry
1	1	16 8-bit character display — Right entry

Controller

For description of right and left entry, see Interface Considerations. Note that when decoded scan is set in keyboard mode, the display is reduced to 4 characters independent of display mode set.

KKK			
0	0	0	Encoded Scan Keyboard — 2 Key Lockout*
0	0	1	Decoded Scan Keyboard — 2-Key Lockout
0	1	0	Encoded Scan Keyboard — N-Key Rollover
0	1	1	Decoded Scan Keyboard — N-Key Rollover
1	0	0	Encoded Scan Sensor Matrix
1	0	1	Decoded Scan Sensor Matrix
1	1	0	Strobed Input, Encoded Display Scan
1	1	1	Strobed Input, Decoded Display Scan

Controller

Program Clock

Code:	0	0	1	P	P	P	P	P

All timing and multiplexing signals for the 8279 are generated by an internal prescaler. This prescaler divides the external clock (pin 3) by a programmable integer. Bits PPPPP determine the value of this integer which ranges from 2 to 31. Choosing a divisor that yields 100 kHz will give the specified scan and debounce times. For instance, if Pin 3 of the 8279 is being clocked by a 2 MHz signal, PPPPP should be set to 10100 to divide the clock by 20 to yield the proper 100 kHz operating frequency.

use divisor = 2 and clock rate (153600 Hz) for 77 kHz scan rate

Read FIFO/Sensor RAM

Code:	0	1	0	AI	X	A	A	A	X = Don't Care

The CPU sets up the 8279 for a read of the FIFO/Sensor RAM by first writing this command. In the Scan Key-

---

*Default after reset

Scan key-board Mode, the Auto-Increment flag (AI) and the RAM address bits (AAA) are irrelevant. The 8279 will automatically drive the data bus for each subsequent read ($A_0 = 0$) in the same sequence in which the data first entered the FIFO. All subsequent reads will be from the FIFO until another command is issued.

In the Sensor Matrix Mode, the RAM address bits AAA select one of the 8 rows of the Sensor RAM. If the AI flag is set (AI = 1), each successive read will be from the subsequent row of the sensor RAM.

Controller - DO NOT USE
only read FIFO
Keep display in RAM if needed

Read Display RAM

Code:

0	1	1	AI	A	A	A	A

The CPU sets up the 8279 for a read of the Display RAM by first writing this command. The address bits AAAA select one of the 16 rows of the Display RAM. If the AI flag is set (AI = 1), this row address will be incremented after each following read *or write* to the Display RAM. Since the same counter is used for both reading and writing, this command sets the next read *or write* address and the sense of the Auto-Increment mode for both operations.

Write Display RAM

Code:

1	0	0	AI	A	A	A	A

The CPU sets up the 8279 for a write to the Display RAM by first writing this command. After writing the command with $A_0 = 1$, all subsequent writes with $A_0 = 0$ will be to the Display RAM. The addressing and Auto-Increment functions are identical to those for the Read Display RAM. However, this command does not affect the source of subsequent Data Reads; the CPU will read from whichever RAM (Display or FIFO/Sensor) which was last specified. If, indeed, the Display RAM was last specified, the Write Display RAM will, nevertheless, change the next Read location.

NIBBLE

Display Write Inhibit/Blanking

Code:

				A	B	A	B
1	0	1	X	IW	IW	BL	BL

The IW Bits can be used to mask nibble A and nibble B in applications requiring separate 4-bit display ports. By setting the IW flag (IW = 1) for one of the ports, the port becomes marked so that entries to the Display RAM from the CPU do not affect that port. Thus, if each nibble is input to a BCD decoder, the CPU may write a digit to the Display RAM without affecting the other digit being displayed. It is important to note that bit B_0 corresponds to bit D_0 on the CPU bus, and that bit A_3 corresponds to bit D_7.

If the user wishes to blank the display, the BL flags are available for each nibble. The last Clear command issued determines the code to be used as a "blank." This code defaults to all zeros after a reset. Note that both BL flags must be set to blank a display formatted with a single 8-bit port.

Clear

Code:

1	1	0	C_D	C_D	C_D	C_F	C_A

The C_D bits are available in this command to clear all rows of the Display RAM to a selectable blanking code as follows:

C_D	C_D	C_D		
	0	X	All Zeros (X = Don't Care)	OFF
	1	0	AB = Hex 20 (0010 0000)	
	1	1	All Ones	ON

Enable clear display when = 1 (or by C_A = 1)

During the time the Display RAM is being cleared (~160 μs), it may not be written to. The most significant bit of the FIFO status word is set during this time. When the Display RAM becomes available again, it automatically resets.

If the C_F bit is asserted ($C_F = 1$), the FIFO status is cleared and the interrupt output line is reset. Also, the Sensor RAM pointer is set to row 0.

C_A, the Clear All bit, has the combined effect of C_D and C_F; it uses the C_D clearing code on the Display RAM and also clears FIFO status. Furthermore, it resynchronizes the internal timing chain.

End Interrupt/Error Mode Set

Code:

1	1	1	E	X	X	X	X

X = Don't care.

For the sensor matrix modes this command lowers the IRQ line and enables further writing into RAM. (The IRQ line would have been raised upon the detection of a change in a sensor value. This would have also inhibited further writing into the RAM until reset).

For the N-key rollover mode — if the E bit is programmed to "1" the chip will operate in the special Error mode. (For further details, see Interface Considerations Section.)

Status Word - FIFO

The status word contains the FIFO status, error, and display unavailable signals. This word is read by the CPU when A_0 is high and $\overline{CS}$ and $\overline{RD}$ are low. See Interface Considerations for more detail on status word.

Data Read

C/D

Data is read when A_0, $\overline{CS}$ and $\overline{RD}$ are all low. The source of the data is specified by the Read FIFO or Read Display commands. The trailing edge of $\overline{RD}$ will cause the address of the RAM being read to be incremented if the Auto-Increment flag is set. FIFO reads always increment (if no error occurs) independent of AI.

Data Write

C/D

Data that is written with A_0, $\overline{CS}$ and $\overline{WR}$ low is always written to the Display RAM. The address is specified by the latest Read Display or Write Display command. Auto-Incrementing on the rising edge of $\overline{WR}$ occurs if AI set by the latest display command.

using shift/control to encode 4 scan lines causes Depressed key to appear only every 16th scan state, not every 8th — this means debouncing test every scan fails - must be every other. For 2key lockout, doesn't say if checks every 8.

P.28 says OK

INTERFACE CONSIDERATIONS

Controller

Scanned Keyboard Mode, 2-Key Lockout

There are three possible combinations of conditions that can occur during debounce scanning. When a key is depressed, the debounce logic is set. Other depressed keys are looked for during the next two scans. If none are encountered, it is a single key depression and the key position is entered into the FIFO along with the status of CNTL and SHIFT lines. If the FIFO was empty, IRQ will be set to signal the CPU that there is an entry in the FIFO. If the FIFO was full, the key will not be entered and the error flag will be set. If another closed switch is encountered, no entry to the FIFO can occur. If all other keys are released before this one, then it will be entered to the FIFO. If this key is released before any other, it will be entirely ignored. A key is entered to the FIFO only once per depression, no matter how many keys were pressed along with it or in what order they were released. If two keys are depressed within the debounce cycle, it is a simultaneous depression. Neither key will be recognized until one key remains depressed alone. The last key will be treated as a single key depression.

Scanned Keyboard Mode, N-Key Rollover

With N-key Rollover each key depression is treated independently from all others. When a key is depressed, the debounce circuit waits 2 keyboard scans and then checks to see if the key is still down. If it is, the key is entered into the FIFO. Any number of keys can be depressed and another can be recognized and entered into the FIFO. If a simultaneous depression occurs, the keys are recognized and entered according to the order the keyboard scan found them.

N Key Rollover

Scanned Keyboard — Special Error Modes

For N-key rollover mode the user can program a special error mode. This is done by the "End Interrupt/Error Mode Set" command. The debounce cycle and key-validity check are as in normal N-key mode. If during a single debounce cycle, two keys are found depressed, this is considered a simultaneous multiple depression, and sets an error flag. This flag will prevent any further writing into the FIFO and will set interrupt (if not yet set). The error flag could be read in this mode by reading the FIFO STATUS word. (See "FIFO STATUS" for further details.) The error flag is reset by sending the normal CLEAR command with $C_F = 1$.

Sensor Matrix Mode

In Sensor Matrix mode, the debounce logic is inhibited. The status of the sensor switch is inputted directly to the Sensor RAM. In this way the Sensor RAM keeps an image of the state of the switches in the sensor matrix. Although debouncing is not provided, this mode has the advantage that the CPU knows how long the sensor was closed and when it was released. A keyboard mode can only indicate a validated closure. To make the software easier, the designer should functionally group the sensors by row since this is the format in which the CPU will read them.

The IRQ line goes high if any sensor value change is detected at the end of a sensor matrix scan. The IRQ line is cleared by the first data read operation if the Auto-Increment flag is set to zero, or by the End Interrupt command if the Auto-Increment flag is set to one.

Note: Multiple changes in the matrix Addressed by (SL_{0-3} = 0) may cause multiple interrupts. (SL_0 = 0 in the Decoded Mode). Reset may cause the 8279 to see multiple changes.

Data Format

In the Scanned Keyboard mode, the character entered into the FIFO corresponds to the position of the switch in the keyboard plus the status of the CNTL and SHIFT lines (non-inverted). CNTL is the MSB of the character and SHIFT is the next most significant bit. The next three bits are from the scan counter and indicate the row the key was found in. The last three bits are from the column counter and indicate to which return line the key was connected.

MSB				LSB
CNTL	SHIFT	SCAN		RETURN

SCANNED KEYBOARD DATA FORMAT

In Sensor Matrix mode, the data on the return lines is entered directly in the row of the Sensor RAM that corresponds to the row in the matrix being scanned. Therefore, each switch postion maps directly to a Sensor RAM position. The SHIFT and CNTL inputs are ignored in this mode. Note that switches are not necessarily the only thing that can be connected to the return lines in this mode. Any logic that can be triggered by the scan lines can enter data to the return line inputs. Eight multiplexed input ports could be tied to the return lines and scanned by the 8279.

MSB							LSB
RL_7	RL_6	RL_5	RL_4	RL_3	RL_2	RL_1	RL_0

In Strobed Input mode, the data is also entered to the FIFO from the return lines. The data is entered by the rising edge of a CNTL/STB line pulse. Data can come from another encoded keyboard or simple switch matrix. The return lines can also be used as a general purpose strobed input.

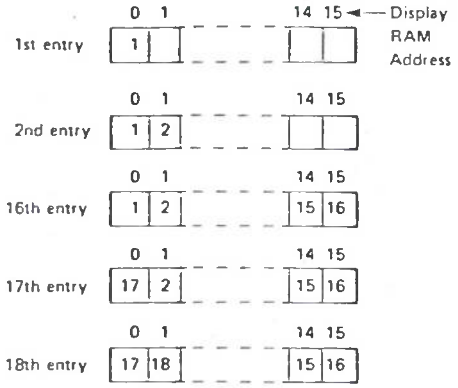
MSB							LSB
RL_7	RL_6	RL_5	RL_4	RL_3	RL_2	RL_1	RL_0

Display

Controller

Left Entry

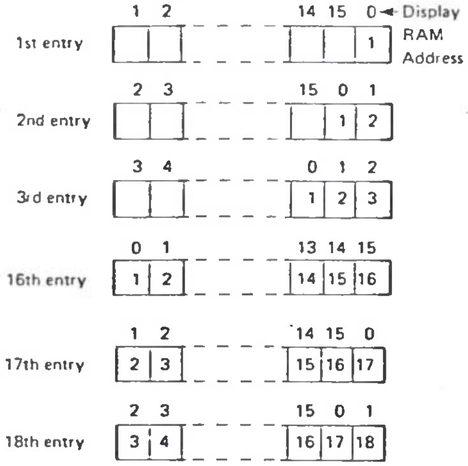
Left Entry mode is the simplest display format in that each display position directly corresponds to a byte (or nibble) in the Display RAM. Address 0 in the RAM is the left-most display character and address 15 (or address 7 in 8 character display) is the right most display character. Entering characters from position zero causes the display to fill from the left. The 17th (9th) character is entered back in the left most position and filling again proceeds from there.



LEFT ENTRY MODE
(AUTO INCREMENT)

Right Entry

Right entry is the method used by most electronic calculators. The first entry is placed in the right most display character. The next entry is also placed in the right most character after the display is shifted left one character. The left most character is shifted off the end and is lost.

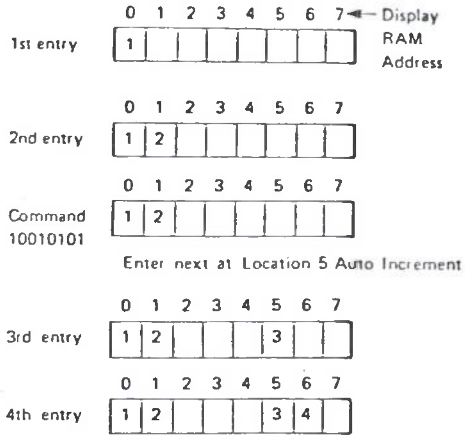


RIGHT ENTRY MODE
(AUTO INCREMENT)

Note that now the display position and register address do not correspond. Consequently, entering a character to an arbitrary position in the Auto Increment mode may have unexpected results. Entry starting at Display RAM address 0 with sequential entry is recommended.

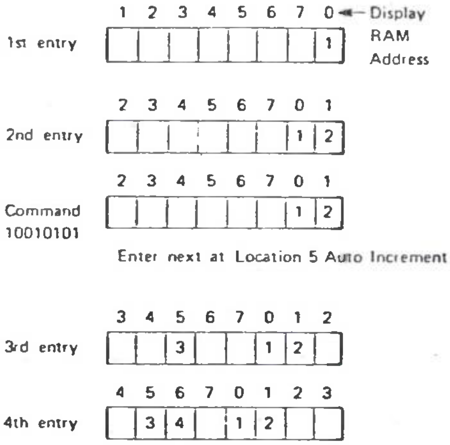
Auto Increment

In the Left Entry mode, Auto Incrementing causes the address where the CPU will next write to be incremented by one and the character appears in the next location. With non-Auto Incrementing the entry is both to the same RAM address and display position. Entry to an arbitrary address in the Auto Increment mode has no undesirable side effects and the result is predictable:



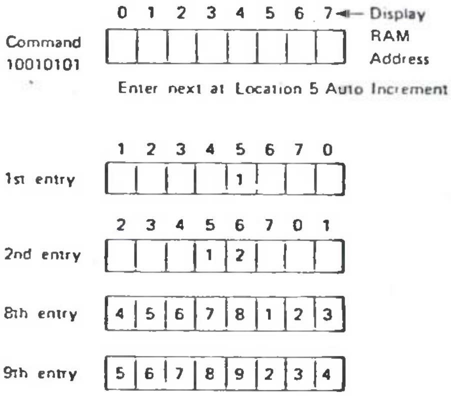
LEFT ENTRY MODE
(AUTO INCREMENT)

In the Right Entry mode, Auto Incrementing and non Incrementing have the same effect as in the Left Entry except if the address sequence is interrupted:



RIGHT ENTRY MODE
(AUTO INCREMENT)

Starting at an arbitrary location operates as shown below:



RIGHT ENTRY MODE
(AUTO INCREMENT)

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Entry appears to be from the initial entry point.

8/16 Character Display Formats

If the display mode is set to an 8 character display, the on duty-cycle is double what it would be for a 16 character display (e.g., 5.1 ms scan time for 8 characters vs. 10.3 ms for 16 characters with 100 kHz internal frequency).

G. FIFO Status

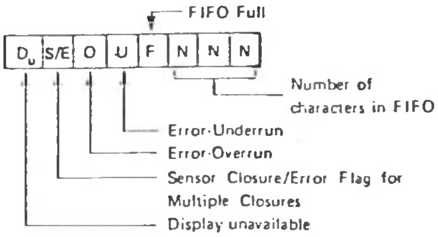
FIFO status is used in the Keyboard and Strobed Input modes to indicate the number of characters in the FIFO and to indicate whether an error has occurred. There are two types of errors possible: overrun and underrun. Overrun occurs when the entry of another character into a full FIFO is attempted. Underrun occurs when the CPU tries to read an empty FIFO.

The FIFO status word also has a bit to indicate that the Display RAM was unavailable because a Clear Display or Clear All command had not completed its clearing operation.

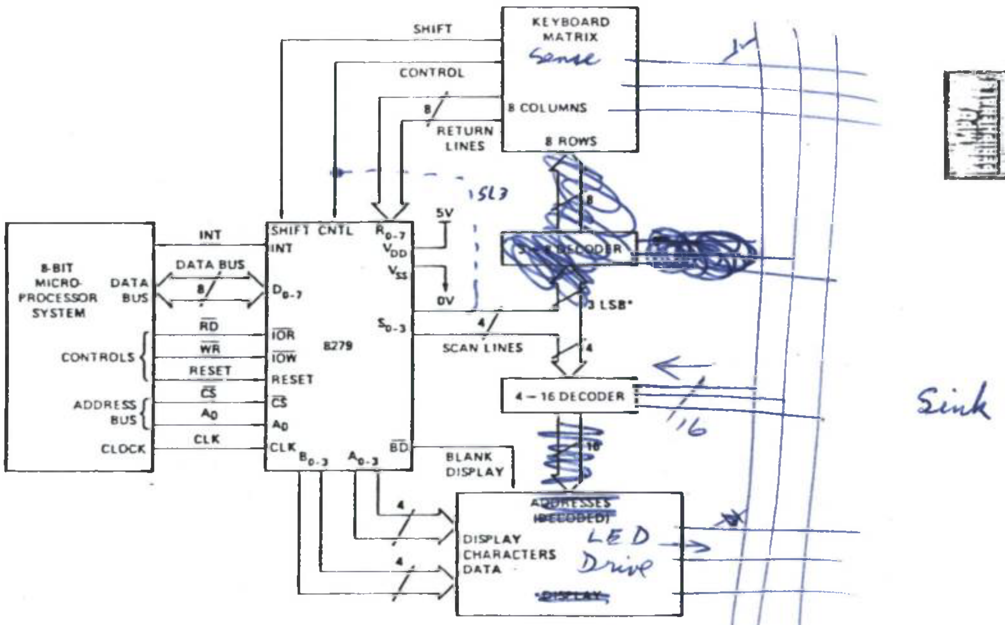
In a Sensor Matrix mode, a bit is set in the FIFO status word to indicate that at least one sensor closure indication is contained in the Sensor RAM.

In Special Error Mode the S/E bit is showing the error flag and serves as an indication to whether a simultaneous multiple closure error has occurred.

FIFO STATUS WORD


FIFO Full
D_u
S/E
O
U
F
N
N
N
Number of characters in FIFO
Error-Underrun
Error-Overrun
Sensor Closure/Error Flag for Multiple Closures
Display unavailable

APPLICATIONS



*Do not drive the keyboard decoder with the MSB of the scan lines.

however, can use MSB scan line to go to shift or Control, then can decode all 4 for KB

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ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Voltage on any Pin with Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{SS} = 0V$, $V_{CC} = +5V \pm 5\%$; $V_{CC} = +5V \pm 10\%$ (8279-5)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL1}	Input Low Voltage for Return Lines	-0.5	1.4	V	
V_{IL2}	Input Low Voltage for All Others	-0.5	0.8	V	
V_{IH1}	Input High Voltage for Return Lines	2.2		V	
V_{IH2}	Input High Voltage for All Others	2.0		V	
V_{OL}	Output Low Voltage		0.45	V	Note 1
V_{OH1}	Output High Voltage on Interrupt Line	3.5		V	Note 2
V_{OH2}	Other Outputs	2.4			
I_{IL1}	Input Current on Shift, Control and Return Lines		+10 -100	μA μA	$V_{IN} = V_{CC}$ $V_{IN} = 0V$
I_{IL2}	Input Leakage Current on All Others		±10	μA	$V_{IN} = V_{CC}$ to 0V
I_{OFL}	Output Float Leakage		±10	μA	$V_{OUT} = V_{CC}$ to 0V
I_{CC}	Power Supply Current		120	mA	

Notes:

8279, I_{OL} = 1.6mA; 8279-5, I_{OL} = 2.2mA.

8279, I_{OH} = -100μA; 8279-5, I_{OH} = -400μA.

CAPACITANCE

SYMBOL	TEST	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{in}	Input Capacitance	5	10	pF	$V_{in}=V_{CC}$
C_{out}	Output Capacitance	10	20	pF	$V_{out}=V_{CC}$

A.C. CHARACTERISTICS

$T_A = 0^\circ C$ to $70^\circ C$, $V_{SS} = 0V$, (Note 1)

Bus Parameters

Read Cycle:

Symbol	Parameter	8279		8279-5		Unit
		Min.	Max.	Min.	Max.	
t_{AR}	Address Stable Before $\overline{\text{READ}}$	50		0		ns
t_{RA}	Address Hold Time for $\overline{\text{READ}}$	5		0		ns
t_{RR}	$\overline{\text{READ}}$ Pulse Width	420		250		ns
t_{RD}[2]	Data Delay from $\overline{\text{READ}}$		300		150	ns
t_{AD}[2]	Address to Data Valid		450		250	ns
t_{DF}	$\overline{\text{READ}}$ to Data Floating	10	100	10	100	ns
t_{RCY}	Read Cycle Time	1		1		μs

Write Cycle:

Symbol	Parameter	8279		8279-5		Unit
		Min.	Max.	Min.	Max.	
t_{AW}	Address Stable Before $\overline{\text{WRITE}}$	50		0		ns
t_{WA}	Address Hold Time for $\overline{\text{WRITE}}$	20		0		ns
t_{WW}	$\overline{\text{WRITE}}$ Pulse Width	400		250		ns
t_{DW}	Data Set Up Time for $\overline{\text{WRITE}}$	300		150		ns
t_{WD}	Data Hold Time for $\overline{\text{WRITE}}$	40		0		ns
t_{WCY}	Write Cycle Time	1		1		μs

Notes:

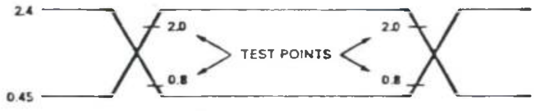
1. 8279, $V_{CC} = +5V \pm 5\%$; 8279-5, $V_{CC} = +5V \pm 10\%$.
2. 8279, $C_L = 100pF$; 8279-5, $C_L = 150pF$.

Other Timings:

Symbol	Parameter	8279		8279-5		Unit
		Min.	Max.	Min.	Max.	
$t_{\phi W}$	Clock Pulse Width	230		120		nsec
t_{CY}	Clock Period	500		320		nsec

Keyboard Scan Time:	5.1 msec	Digit-on Time:	480 μsec
Keyboard Debounce Time:	10.3 msec	Blanking Time:	160 μsec
Key Scan Time:	80 μsec	Internal Clock Cycle:	10 μsec
Display Scan Time:	10.3 msec		

Input Waveforms For A.C. Tests



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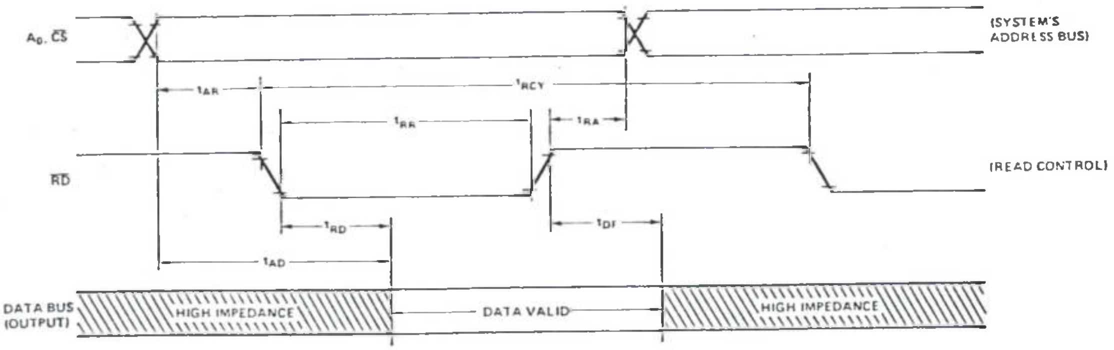
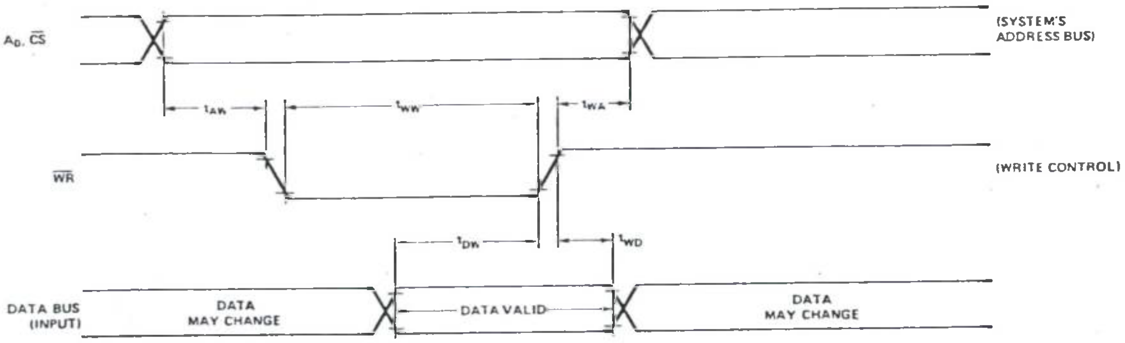
WAVEFORMS

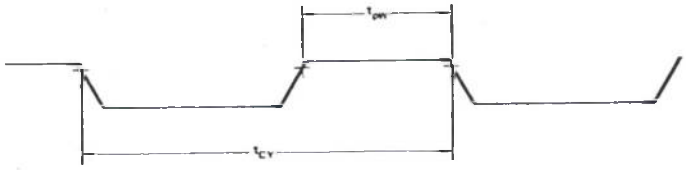
Read Operation



Write Operation



Clock Input



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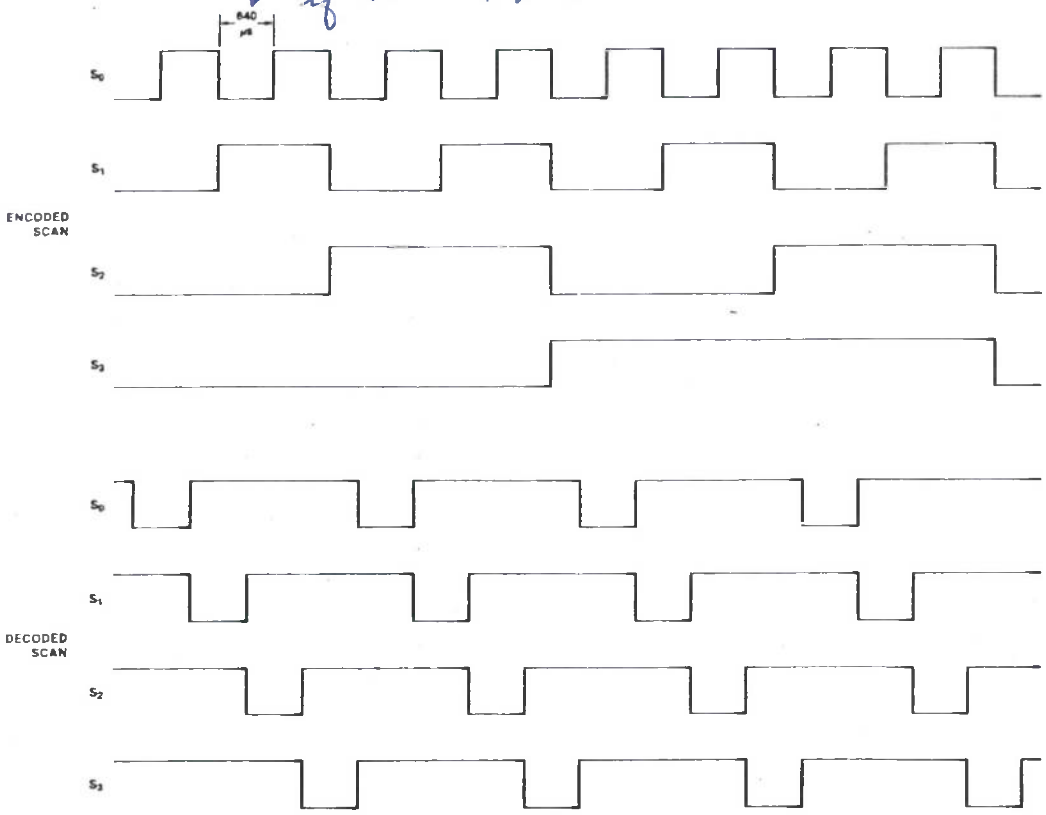
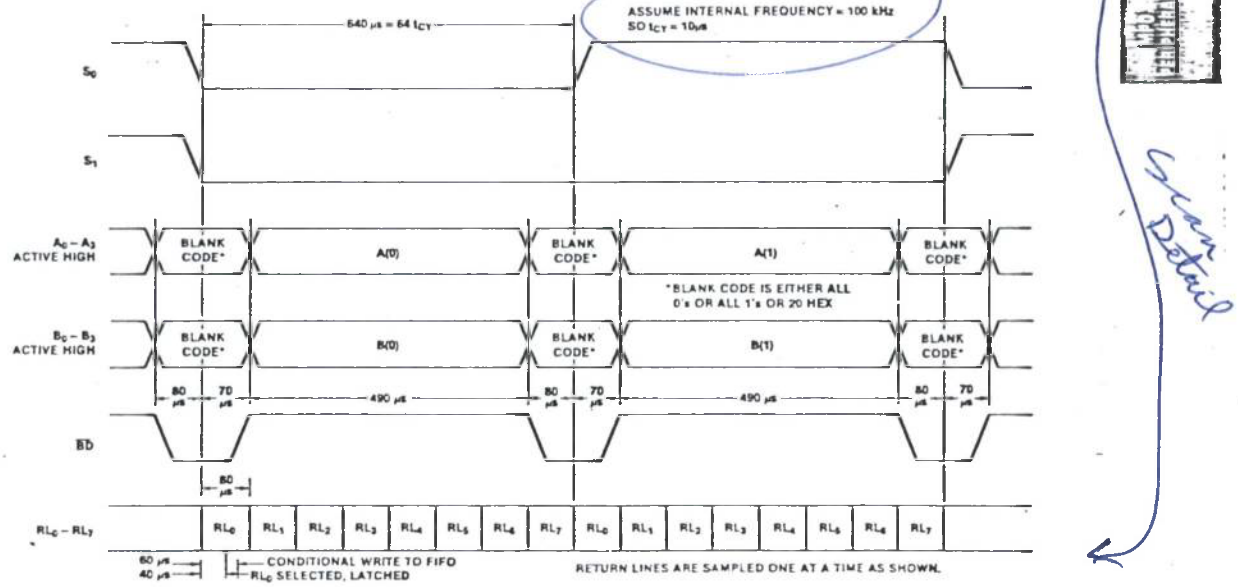
8279 SCAN TIMING

SCAN WAVEFORMS

if internal freq = 100KHz



DISPLAY WAVEFORMS



NOTE: SHOWN IS ENCODED SCAN LEFT ENTRY
S_2-S_3 ARE NOT SHOWN BUT THEY ARE SIMPLY S_1 DIVIDED BY 2 AND 4

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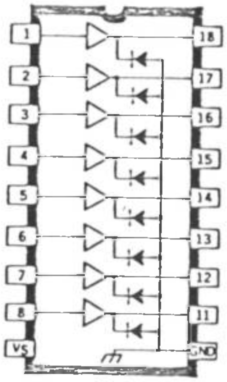
SERIES UDN-2980A
HIGH-VOLTAGE, HIGH-CURRENT SOURCE DRIVERS

RECOMMENDED for applications requiring separate logic and load grounds, load supply voltages to +80 V, and/or load currents to 500 mA, Series UDN-2980A source drivers are used to interface between standard low-power digital logic and relays, solenoids, stepping motors, LEDs, lamps, etc.

Under normal operating conditions, these devices will sustain 100 mA continuously on each of the eight outputs at an ambient temperature of +70°C and a supply of +15 V. All devices in this series incorporate input current limiting resistors and output transient suppression diodes.

The Type UDN-2981A and UDN-2983A drivers are for use with +5 V logic systems — TTL, Schottky TTL, DTL, and 5 V CMOS. The Type UDN-2982A and UDN-2984A drivers are intended for MOS interface (PMOS and CMOS) operating from supply voltages of 6 to 16 V. The UDN-2981A and UDN-2982A will sustain a maximum output OFF voltage of +50 V while the UDN-2983A and UDN-2984A will sustain an output voltage of +80 V. In all cases, the output is switched ON by an active high input level.

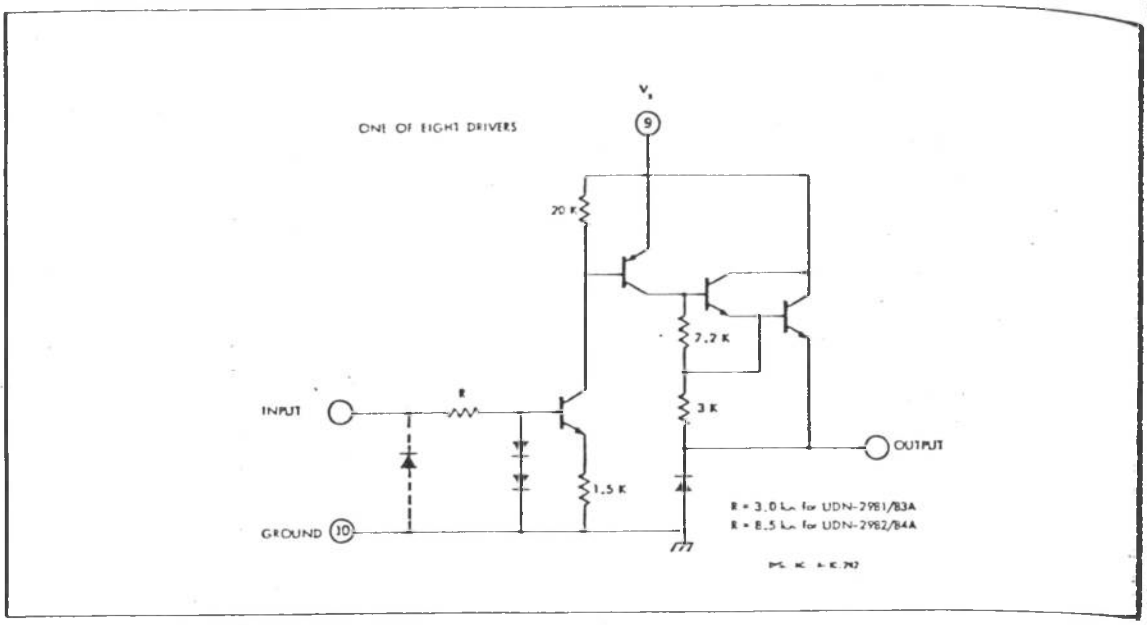
The Series UDN-2980A high-voltage, high-current source drivers are supplied in 18-lead dual in-line plastic packages. They can also be supplied, with reduced package power capability, in military-grade hermetic packages to the processing and environmental requirements of Military Standard MIL-STD-883, or industrial-grade dual in-line hermetic packages. To order, change the last letter of the part number from 'A' to 'H' or 'R', respectively.



ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature

Output Voltage, V_{CE}	(UDN-2981A & UDN-2982A)	+50 V
	(UDN-2983A & UDN-2984A)	+80 V
Input Voltage, V_{IN}	(UDN-2981A & UDN-2983A)	+15 V
	(UDN-2982A & UDN-2984A)	+30 V
Output Current, I_{OUT}		−500 mA
Power Dissipation, P_D	(any one driver)	1.1 W
	(total package)	2.2 W*
Operating Temperature Range, T_A		0°C to +70°C
Storage Temperature Range, T_S		−55°C to +150°C

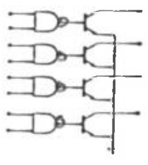
*Derate at the rate of 18 mW/°C above 25°C.

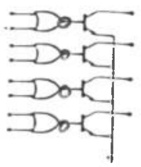


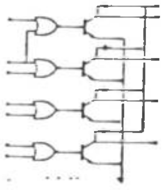
ELECTRICAL CHARACTERISTICS at T_A = +25°C (unless otherwise specified)

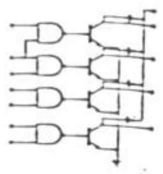
Characteristic	Symbol	Applicable Devices	Test Conditions	Limit
Output Leakage Current	I_{CEX}	UDN-2981/82A	V_{IN} = 0.4 V, V_S = 50 V, T_A = +70°C	200 μA Max
		UDN-2983/84A	V_{IN} = 0.4 V, V_S = 80 V, T_A = +70°C	200 μA Max
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	UDN-2981/83A	V_{IN} = 2.4 V, I_{OUT} = −100 mA	1.7 V Max
			V_{IN} = 2.4 V, I_{OUT} = −225 mA	1.8 V Max
			V_{IN} = 2.4 V, I_{OUT} = −350 mA	1.9 V Max
		UDN-2982/84A	V_{IN} = 5.0 V, I_{OUT} = −100 mA	1.7 V Max
			V_{IN} = 5.0 V, I_{OUT} = −225 mA	1.8 V Max
			V_{IN} = 5.0 V, I_{OUT} = −350 mA	1.9 V Max
Input Current	$I_{IN(ON)}$	UDN-2981/83A	V_{IN} = 2.4 V	575 μA Max
			V_{IN} = 3.85 V	1.26 mA Max
		UDN-2982/84A	V_{IN} = 5.0 V	680 μA Max
			V_{IN} = 12 V	1.93 mA Max
Output Source Current	I_{OUT}	UDN-2981/83A	V_{IN} = 2.4 V, V_{CE} = 2.0 V	−350 mA Max
		UDN-2982/84A	V_{IN} = 5.0 V, V_{CE} = 2.0 V	−350 mA Max
Supply Current (Outputs Open)	I_S	UDN-2981A	V_{IN} = 2.4 V (All Inputs), V_S = 50 V	10 mA Max
		UDN-2982A	V_{IN} = 5.0 V (All Inputs), V_S = 50 V	10 mA Max
		UDN-2983A	V_{IN} = 2.4 V (All Inputs), V_S = 80 V	10 mA Max
		UDN-2984A	V_{IN} = 5.0 V (All Inputs), V_S = 80 V	10 mA Max
Clamp Diode Leakage Current	I_R	UDN-2981/82A	V_R = 50 V, V_{IN} = 0 V	50 μA Max
		UDN-2983/84A	V_R = 80 V, V_{IN} = 0 V	50 μA Max
Clamp Diode Forward Voltage	V_F	ALL	I_F = 350 mA	2.0 V Max

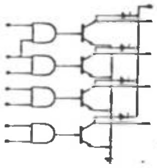
SERIES UHP-400, UHP-400-1, & UHP-500 POWER and RELAY DRIVERS — PLASTIC ENCASED

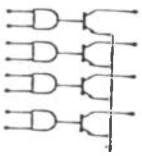

UHP-400/400-1/500
Quad 2 AND

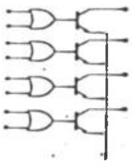

UHP-402/402-1/502
Quad 2 OR

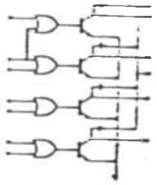

UHP-403/403-1/503
Quad OR


UHP-406/406-1/506
Quad AND


UHP-407/407-1/507
Quad NAND


UHP-408/408-1/508
Quad 2 NAND


UHP-432/432-1/532
Quad 2 NOR


UHP-433/433-1/533
Quad NOR

FEATURES

- Inputs Compatible with DTL/TTL
- 500mA Output Sink Current Capability
- Pinning Compatible with 54/74 Logic Series
- Transient Protected Outputs on Relay Drivers
- High Voltage Output – 100V Series UHP-500, 70V Series UHP-400-1, 40V Series UHP-400

Description

These power and relay drivers are bi-polar monolithic circuits and incorporate logic gates and high-current switching transistors on the same chip. Each output transistor is capable of sinking 500mA in the ON state. In the OFF state, Series UHP-400 devices will sustain 40V, Series UHP-400-1 devices will sustain 70V, and Series UHP-500 devices will sustain 100V.

Applications

The UHP-400, UHP-400-1, and UHP-500 Series Power Drivers are ideally suited for driving incandescent lamps, relays, solenoids, and other interface devices with up to 1A output current per package.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7V
Input Voltage, V_{in}:	5.5V
Output Off-state Voltage, V_{off}:	
Series UHP-400	40V
Series UHP-400-1	70V
Series UHP-500	100V
Output On-State Sink Current, I_{on}	500mA
Suppression Diode Off-State Voltage, V_{off}.	
Series UHP-400	40V
Series UHP-400-1	70V
Series UHP-500	100V
Suppression Diode On-State Current, I_{on}	500mA
Operating Free-Air Temperature Range, T_A	0°C to +70°C
Storage Temperature Range, T_S	−65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC}):	4.75	5.0	5.25	V
Operating Temperature Range	0	+25	+70	°C
Current into any output (ON state)			250	mA

ELECTRICAL CHARACTERISTICS:
(over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.8	V	
"0" Input Current at all Inputs except Strobe	$I_{in(0)}$		MAX	0.4V	4.5V			−0.55	−0.8	mA	2
"0" Input Current at Strobe	$I_{in(0)}$		MAX	0.4V	4.5V			−1.1	−1.6	mA	
"1" Input Current at all Inputs except Strobe	$I_{in(1)}$		MAX	2.4V	0V				40	μA	2
			MAX	5.5V	0V				1	mA	
"1" Input Current at Strobe	$I_{in(1)}$		MAX	2.4V	0V				100	μA	2
			MAX	5.5V	0V				1	mA	

SWITCHING CHARACTERISTICS: $V_{CC} = 5.0V$, $T_A = 25°C$

Characteristic	Symbol	Test Conditions	Limits				Notes
			Min.	Typ.	Max.	Units	
Turn-on Delay Time Series UHP-400 Series UHP-400-1 Series UHP-500	t_{pd0}	$V_S = 40V$, $R_L = 265\Omega$ (6 Watts) $V_S = 70V$, $R_L = 465\Omega$ (10 Watts) $V_S = 100V$, $R_L = 670\Omega$ (15 Watts) $C_L = 15pF$		200	500	ns	3
Turn-off Delay Time Series UHP-400 Series UHP-400-1 Series UHP-500	t_{pd1}	$V_S = 40V$, $R_L = 265\Omega$ (6 Watts) $V_S = 70V$, $R_L = 465\Omega$ (10 Watts) $V_S = 100V$, $R_L = 670\Omega$ (15 Watts) $C_L = 15pF$		300	750	ns	3

INPUT PULSE CHARACTERISTICS

$V_{in(0)} = 0V$	$t_f = 7ns$	$t_p = 1\mu s$
$V_{in(1)} = 3.5V$	$t_r = 14ns$	PRR = 500kHz

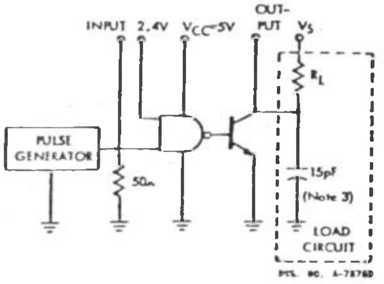
NOTES:

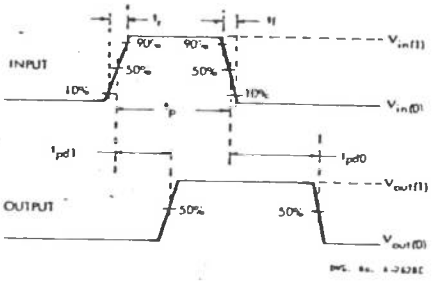
1. Typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

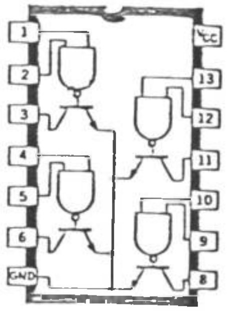
Type UHP-400, UHP-400-1, and UHP-500 Quad 2-Input AND Power Drivers

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current Type UHP-400	I_{off}		MIN	2.0V	2.0V	40V			50	μA	
"1" Output Reverse Current Type UHP-400-1	I_{off}		MIN	2.0V	2.0V	70V			50	μA	
"1" Output Reverse Current Type UHP-500	I_{off}		MIN	2.0V	2.0V	100V			50	μA	
"0" Output Voltage	V_{on}		MIN	0.8V	V_{cc}	150mA			0.5	V	
			MIN	0.8V	V_{cc}	250mA			0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0V	5.0V			4	6	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0V	0V			17.5	24.5	mA	1, 2



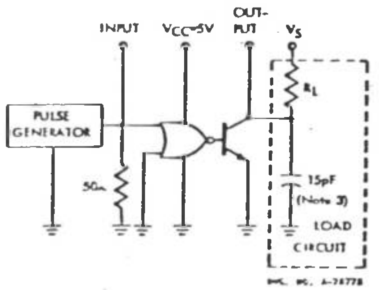


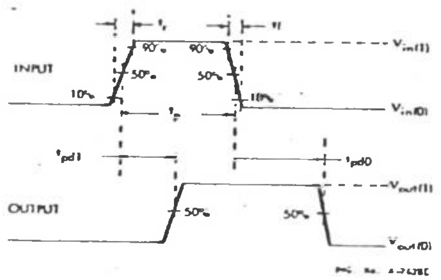


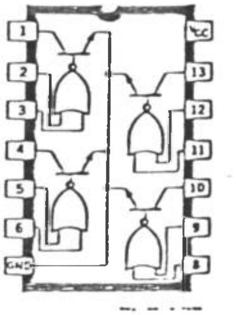
Type UHP-402, UHP-402-1, and UHP-502 Quad 2-Input OR Power Drivers

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current Type UHP-402	I_{off}		MIN	2.0V	0V	40V			50	μA	
"1" Output Reverse Current Type UHP-402-1	I_{off}		MIN	2.0V	0V	70V			50	μA	
"1" Output Reverse Current Type UHP-502	I_{off}		MIN	2.0V	0V	100V			50	μA	
"0" Output Voltage	V_{on}		MIN	0.8V	0.8V	150mA			0.5	V	
			MIN	0.8V	0.8V	250mA			0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0V	5.0V			4.1	6.3	mA	1,2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0V	0V			18	25	mA	1,2







NOTES:

1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each gate.
3. Capacitance values specified include probe and test fixture capacitance.

National Semiconductor

DS1488 quad line driver

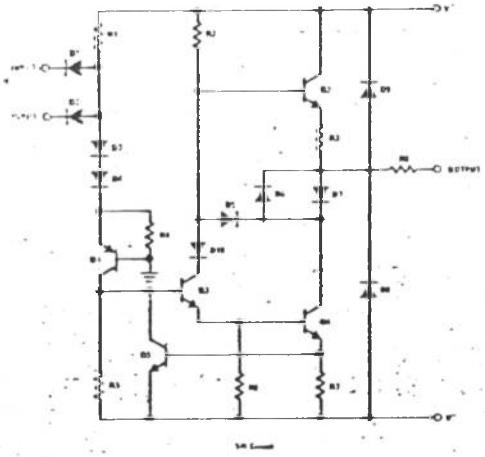
general description

The DS1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V. 24.

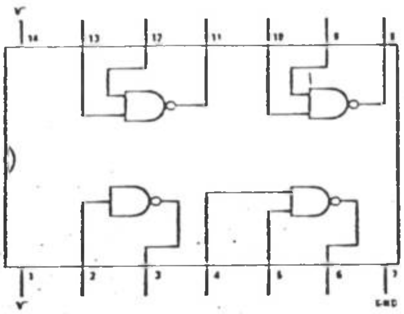
features

- Current limited output ±10 mA typ
- Power-off source impedance 300Ω min
- Simple slew rate control with external capacitor
- Flexible operating supply range
- Inputs are DTL/TTL compatible

schematic and connection diagrams



Dual-In-Line Package

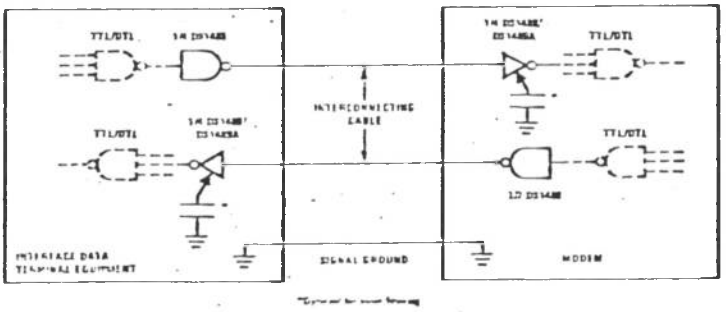


TOP VIEW

Order Number DS1488J or DS1488N
See NS Package J14A or N14A

typical applications

RS232C Data Transmission



absolute maximum ratings (Note 1)

Supply Voltage	
V^+	+15V
V^-	−15V
Input Voltage (V_{IN})	$-15V \le V_{IN} \le 7.0V$
Output Voltage	±15V
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Notes 2, 3 and 4)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	Logical "0" Input Current	$V_{IN} = 0V$			−1.0	−1.3	mA
I_{IH}	Logical "1" Input Current	$V_{IN} = +5.0V$			0.005	10.0	μA
V_{OH}	High Level Output Voltage	$R_L = 3.0\ k\Omega$, $V_{IN} = 0.8V$	$V^+ = 9.0V$, $V^- = -9.0V$	6.0	7.0		V
			$V^+ = 13.2V$, $V^- = -13.2V$	9.0	10.5		V
V_{OL}	Low Level Output Voltage	$R_L = 3.0\ k\Omega$, $V_{IN} = 1.9V$	$V^+ = 9.0V$, $V^- = -9.0V$		−6.8	−6.0	V
			$V^+ = 13.2V$, $V^- = -13.2V$		−10.5	−9.0	V
I_{OS}^+	High Level Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = 0.8V$		−6.0	−10.0	−12.0	mA
I_{OS}^-	Low Level Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = 1.9V$		6.0	10.0	12.0	mA
R_{OUT}	Output Resistance	$V^+ = V^- = 0V$, $V_{OUT} = \pm 2V$		300			Ω
I_{CC}^+	Positive Supply Current (Output Open)	$V_{IN} = 1.9V$	$V^+ = 9.0V$, $V^- = -9.0V$		15.0	20.0	mA
			$V^+ = 12V$, $V^- = -12V$		19.0	25.0	mA
			$V^+ = 15V$, $V^- = -15V$		25.0	34.0	mA
		$V_{IN} = 0.8V$	$V^+ = 9.0V$, $V^- = -9.0V$		4.5	6.0	mA
			$V^+ = 12V$, $V^- = -12V$		5.5	7.0	mA
			$V^+ = 15V$, $V^- = -15V$		8.0	12.0	mA
I_{CC}^-	Negative Supply Current (Output Open)	$V_{IN} = 1.9V$	$V^+ = 9.0V$, $V^- = -9.0V$		−13.0	−17.0	mA
			$V^+ = 12V$, $V^- = -12V$		−18.0	−23.0	mA
			$V^+ = 15V$, $V^- = -16V$		−25.0	−34.0	mA
		$V_{IN} = 0.8V$	$V^+ = 9.0V$, $V^- = -9.0V$		−0.001	−0.015	mA
			$V^+ = 12V$, $V^- = -12V$		−0.001	−0.015	mA
			$V^+ = 15V$, $V^- = -15V$		−0.01	−2.5	mA
P_d	Power Dissipation	$V^+ = 9.0V$, $V^- = -9.0V$			252	333	mW
		$V^+ = 12V$, $V^- = -12V$			444	576	mW

switching characteristics ($V_{CC} = 9V$, $V_{EE} = -9V$, $T_A = 25°C$)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Propagation Delay to a Logical "1"	$R_L = 3.0\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°C$		230	350	ns
t_{pd0}	Propagation Delay to a Logical "0"	$R_L = 3.0\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°C$		70	175	ns
t_r	Rise Time	$R_L = 3.0\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°C$		75	100	ns
t_f	Fall Time	$R_L = 3.0\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°C$		40	75	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +75°C temperature range for the DS1488.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

applications

By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the DS1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

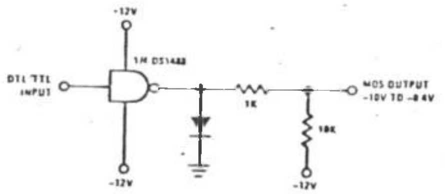
$$C = I_{SC} \ (\Delta T / \Delta V)$$

where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V / \Delta T$ is the slew rate.

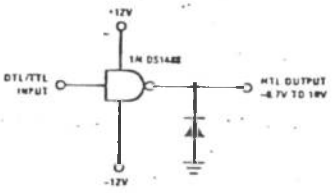
RS232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12 mA in the above equation, calculations result in a required capacitor of 400 pF connected to each output.

typical applications (con't)

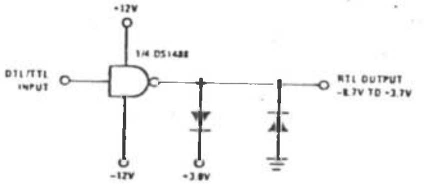
DTL/TTL-to-MOS Translator



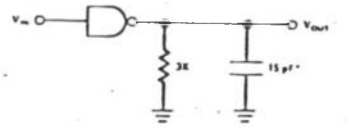
DTL/TTL-to-HTL Translator



DTL/TTL-to-RTL Translator

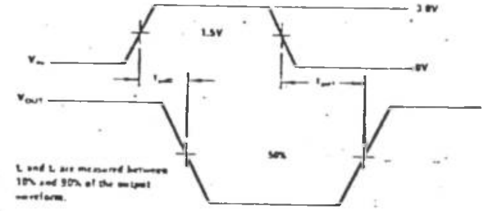


ac load circuit



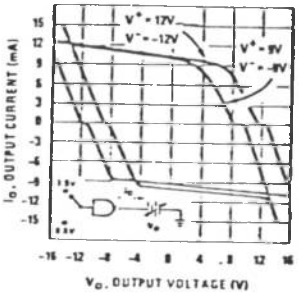
*C_L includes probe and jig capacitance.

switching time waveforms


3.0V
1.5V
V_in
0V
t_pd0
t_pd1
V_OUT
50%
tr and tf are measured between 10% and 90% of the output waveform.

typical performance characteristics

Output Voltage and Current-Limiting Characteristics



54/7400
54H/74H00
54S/74S00
54LS/74LS00

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = -55°C to +125°C
Plastic DIP	Fig. A Fig. A	N7400N • N74H00N N74S00N • N74LS00N	
Ceramic DIP	Fig. A Fig. A	N7400F • N74H00F N74S00F • N74LS00F	S5400F • S54H00F S54S00F • S54LS00F
Flatpak	Fig. B Fig. A		S5400W • S54H00W S54S00W • S54LS00W

PIN CONFIGURATIONS

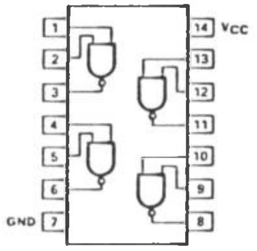


Figure A

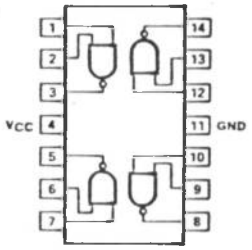


Figure B

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA) I_{IL} (mA)	40 −1.6	50 −2.0	50 −2.0	20 −0.36
Outputs	I_{OH} (μA) I_{OL} (mA)	−400 16	−500 20	−1000 20	−400 4/8 (a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER		TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH}	Supply current	V_{CC} = Max, V_{IN} = 0V		8.0		16.8		16		1.6	mA
I_{CCL}	Supply current	V_{CC} = Max, $V_{IN} \geq$ 4.5V		12		40		36		4.4	mA

AC CHARACTERISTICS T_A = 25°C (See Section 4 for Waveforms and Conditions.)

PARAMETER		TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
			C_L = 15 pF R_L = 400 Ω		C_L = 25 pF R_L = 280 Ω		C_L = 15 pF R_L = 280 Ω		C_L = 15 pF R_L = 2k Ω		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1		22		10		4.5		15	ns
t_{PHL}	Propagation delay	Waveform 1		15		10		5.0		15	ns

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54/74154
54LS/74LS154

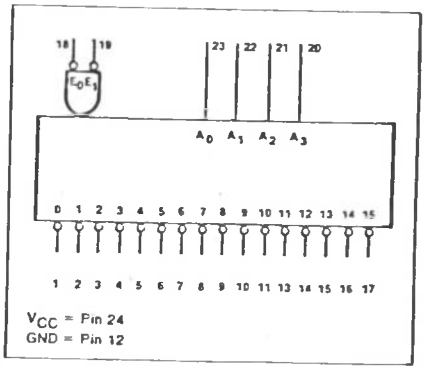
DESCRIPTION

The "154" is a 4-line to 16-line Decoder/Demultiplexer with a 2-input enable gate. It is designed to accept 4-bits of binary data and provide 1-of-16 mutually exclusive active LOW outputs. The enable can be used as a data input to demultiplex up to 16-bits of serial data.

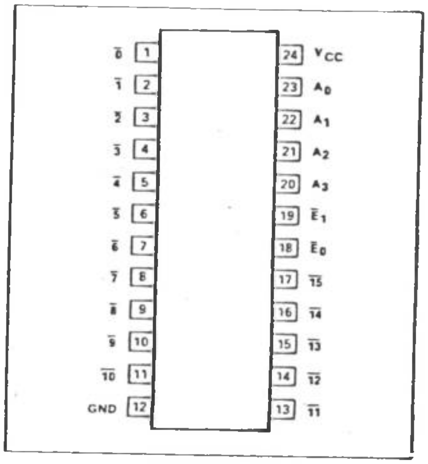
FEATURES

- 16-line demultiplexing capability
- Mutually exclusive outputs
- 2-input enable gate for strobing or expansion

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V_{CC}=5V ± 5%; T_A=0°C to +70°C		MILITARY RANGES V_{CC}=5V ± 10%; T_A=−55°C to +125°C	
Plastic DIP	N74154N	N74LS154N		
Ceramic DIP	N74154F	N74LS154F	S54154F	S54LS154F
Flatpak			S54154W	S54LS154W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE [a]

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
$A_0 - A_3$	Address inputs	I_{IH} (µA) I_{IL} (mA)	40 −1.6		20 −0.36
$\overline{E}_0$, $\overline{E}_1$	Enable (active LOW) inputs	I_{IH} (µA) I_{IL} (mA)	40 −1.6		20 −0.36
$\overline{0} - \overline{15}$	Active LOW outputs	I_{OH} (µA) I_{OL} (mA)	−800 16		−400 4/8[a]

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "154" decoder accepts four active HIGH binary address inputs and provides 16 mutually exclusive active LOW outputs. The 2-input enable gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for expansion of the decoder. The enable gate has two AND'ed inputs which must be LOW to enable the outputs.

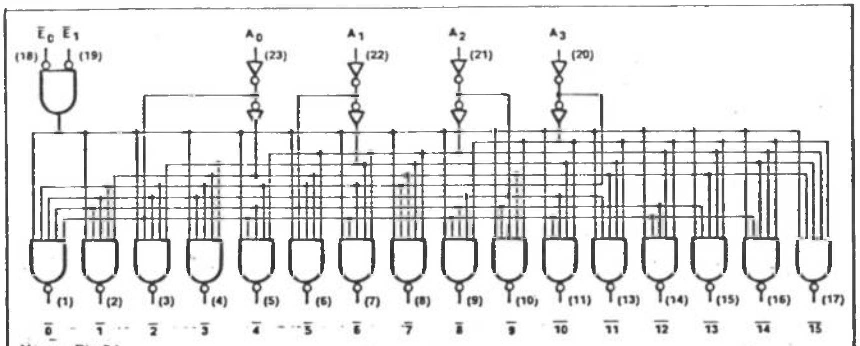
The "154" can be used as a 1-of-16 demultiplexer by using one of the enable inputs as the multiplexed data input. When the other enable is LOW, the addressed output will follow the state of the applied data.

TRUTH TABLE

INPUTS						OUTPUTS															
$\overline{E}_0$	$\overline{E}_1$	A_3	A_2	A_1	A_0	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$	$\overline{10}$	$\overline{11}$	$\overline{12}$	$\overline{13}$	$\overline{14}$	$\overline{15}$
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

LOGIC DIAGRAM



$\overline{E}_0$ $\overline{E}_1$
(18) (19)
A_0 (23)
A_1 (22)
A_2 (21)
A_3 (20)
(1) (2) (3) (4) (5) (6) (7) (8) (9) (10) (11) (13) (14) (15) (16) (17)
$\overline{0}$ $\overline{1}$ $\overline{2}$ $\overline{3}$ $\overline{4}$ $\overline{5}$ $\overline{6}$ $\overline{7}$ $\overline{8}$ $\overline{9}$ $\overline{10}$ $\overline{11}$ $\overline{12}$ $\overline{13}$ $\overline{14}$ $\overline{15}$

V_{CC} = Pin 24
GND = Pin 12
( ) = Pin numbers

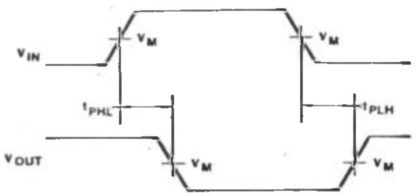
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE[b]

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				Min	Max	Min	Max	Min	Max	
I_{CC}	Supply current	V_{CC} = Max	Mil		49				14	mA
			Com		56				14	mA

AC CHARACTERISTICS: T_A=25°C (See Section 4 for test circuits and conditions)

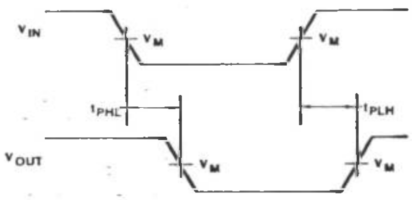
PARAMETER		TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
			C_L = 15pF R_L = 400Ω				C_L = 15pF R_L = 2kΩ		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Figure 1		36 33				36 33	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Figure 2		30 27				30 27	ns ns

AC WAVEFORMS



V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS.

Figure 1



V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS.

Figure 2

NOTE

[b] For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54LS/74LS specification.

CD4000B, CD4001B, CD4002B, CD4025B Types

COS/MOS NOR Gates

High-Voltage Types (20-Volt Rating)

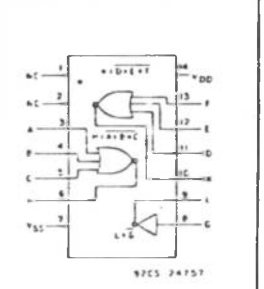
Dual 3 Input
plus Inverter – CD4000B
Quad 2 Input – CD4001B
Dual 4 Input – CD4002B
Triple 3 Input – CD4025B

RCA-CD4000B, CD4001B, CD4002B, and CD4025B NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of COS/MOS gates. All inputs and outputs are buffered.

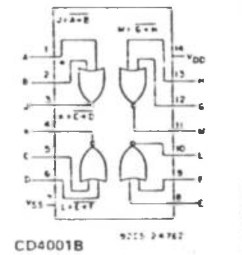
The CD4000B, CD4001B, CD4002B, and CD4025B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Features:

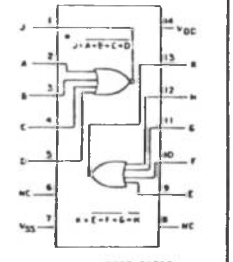
- Propagation delay time = 60 ns (typ.) at C_L = 50 pF, V_{DD} = 10 V
- Buffered inputs and outputs
- Standardized symmetrical output characteristics
- 100% tested for maximum quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  - 1 V at V_{DD} = 5 V
  - 2 V at V_{DD} = 10 V
  - 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of "B" Series CMOS Devices"



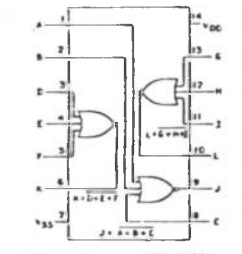
CD4000B
FUNCTIONAL DIAGRAM



CD4001B
FUNCTIONAL DIAGRAM



CD4002B
FUNCTIONAL DIAGRAM



CD4025B
FUNCTIONAL DIAGRAM

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,F,H Packages Values at –40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6		
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8		
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				—	—	1.5	V
	1,9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5	–	5	3.5				3.5	—	—	
	1	–	10	7				7	—	—	
	1.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute Maximum Values*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D)	
For T_A 40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A FULL PACKAGE TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING TEMPERATURE RANGE (T_A)	
PACKAGE TYPES D, F, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max	+265°C

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200kΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5 10 15	125 60 45	250 120 90	ns
Transition Time, t_{THL}, t_{TLH}		5 10 15	100 50 40	200 100 80	ns
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

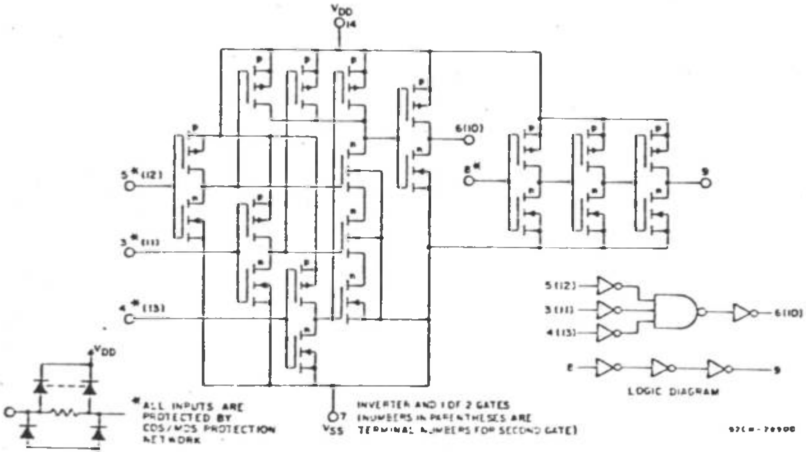

VDD
14
6(10)
8*
9
5*(12)
3*(11)
4*(13)
VDD
VSS
*ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK
7
VSS
INVERTER AND 1 OF 2 GATES (NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR SECOND GATE)
5(12)
3(11)
4(13)
6(10)
8
9
LOGIC DIAGRAM
92CM-29900

Fig.4 – Schematic and logic diagrams for CD4000B.

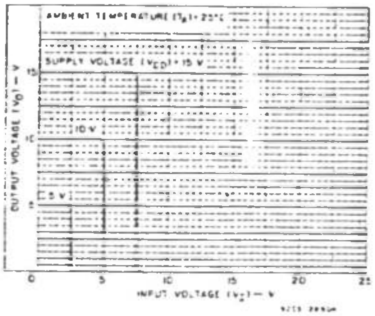


Fig.1 – Typical voltage transfer characteristics.

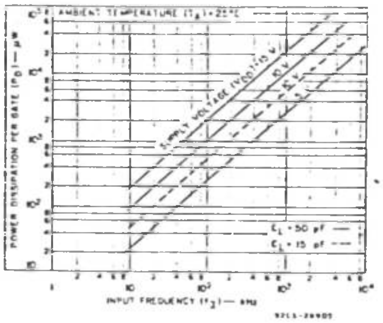


Fig.2 – Typical power dissipation vs. frequency.

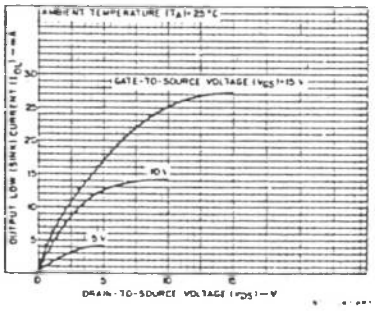


Fig.3 – Typical output low (sink) current characteristics.

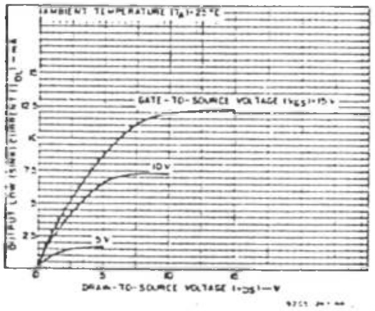
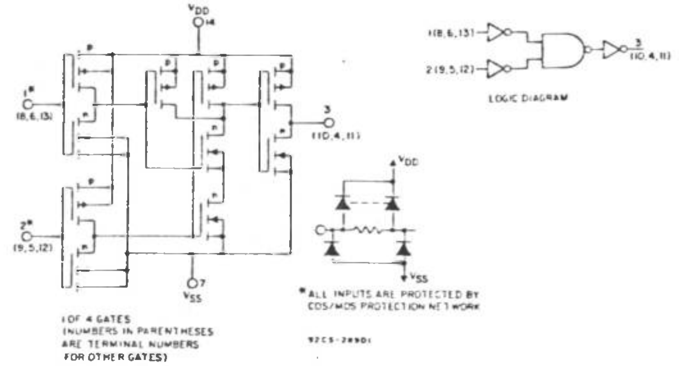


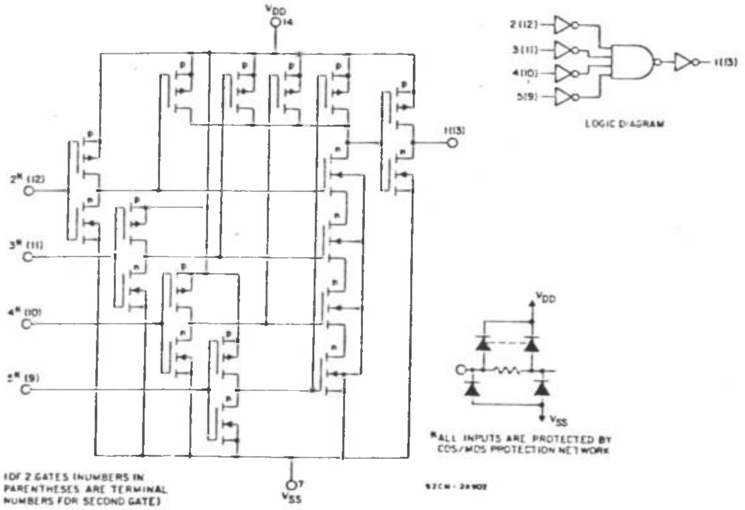
Fig.5 – Minimum output low (sink) current characteristics.



*ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

1 OF 4 GATES
(NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR OTHER GATES)

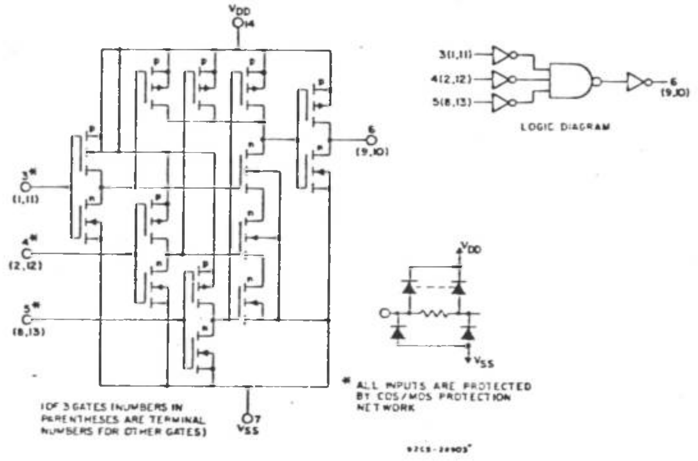
Fig.6 – Schematic and logic diagrams for CD4001B.



*ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

1 OF 2 GATES (NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR SECOND GATE)

Fig.7 – Schematic and logic diagrams for CD4002B.



* ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

1 OF 3 GATES (NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR OTHER GATES)

Fig.8 – Schematic and logic diagrams for CD4025B.

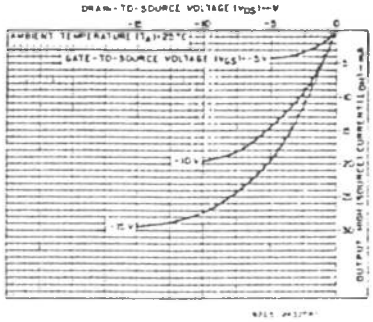


Fig.9 – Typical output high (source) current characteristics.

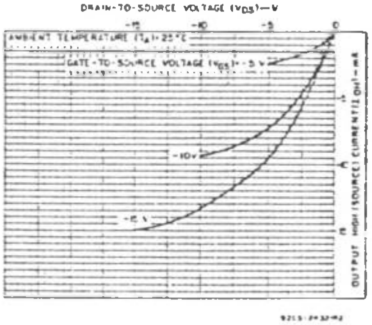


Fig.10 – Minimum output high (source) current characteristics.

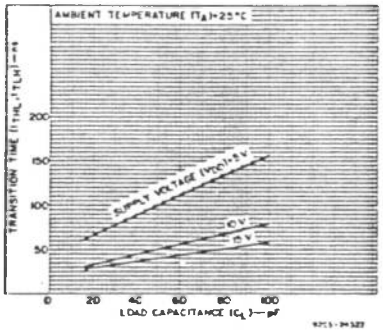


Fig.11 – Typical transition time vs. load capacitance.

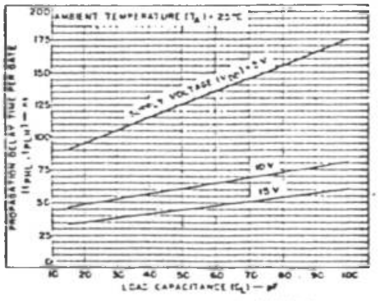


Fig.12 – Typical propagation delay time vs. load capacitance.

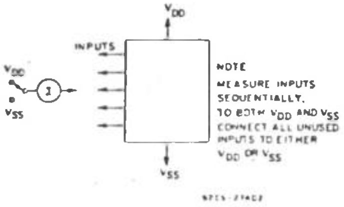

VDD
INPUTS
VDD
VSS
I
NOTE
MEASURE INPUTS SEQUENTIALLY,
TO BOTH VDD AND VSS
CONNECT ALL UNUSED INPUTS TO EITHER VDD OR VSS
VSS
92CS-27402

Fig. 13 – Input leakage current test circuit.

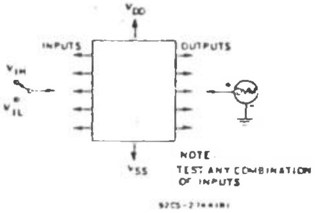


Fig. 14 – Input-voltage test circuit.

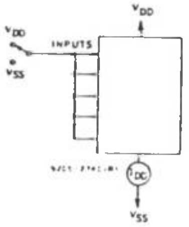
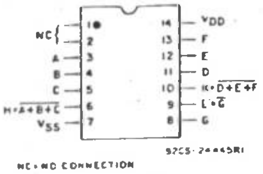
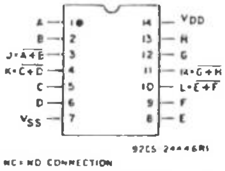


Fig. 15 – Quiescent-device current test circuit.

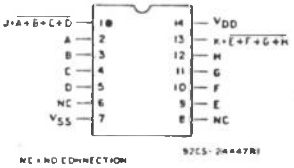
TERMINAL ASSIGNMENTS (TOP VIEW)



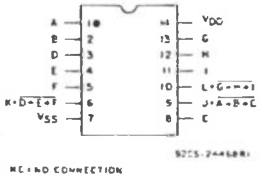
CD4000B



CD4001B



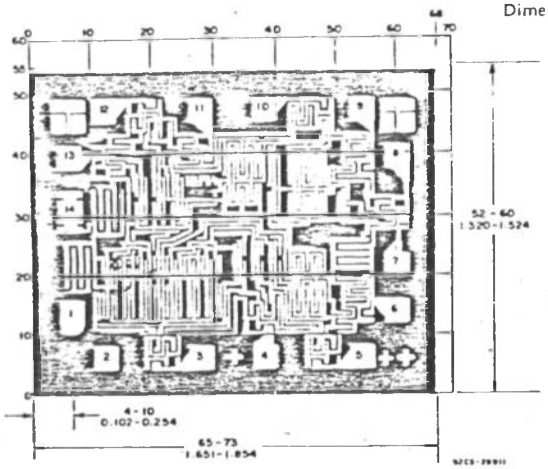
CD4002B



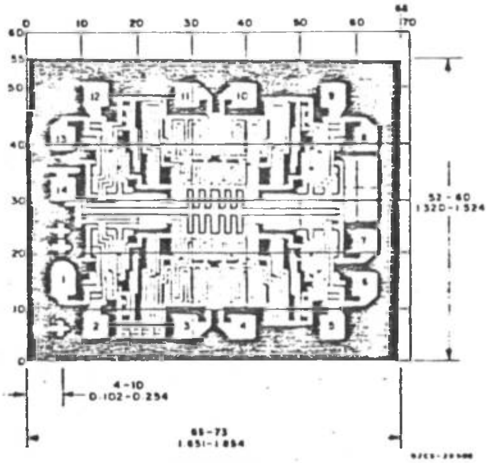
CD4025B

CHIP PHOTOGRAPHS

Dimensions and Pad Layouts



CD4000B



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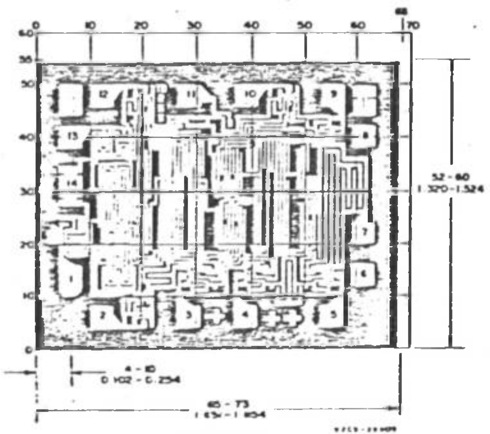
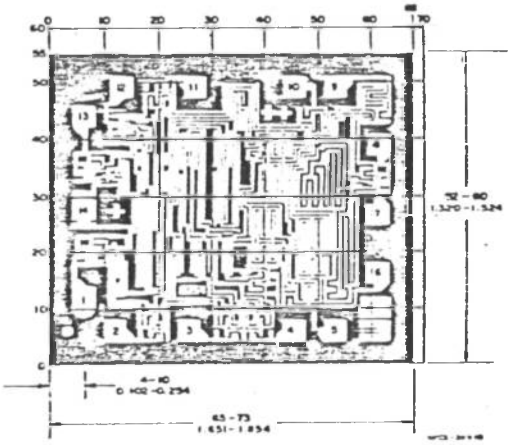


CD4002B



CD4025B

CD4000UB, CD4001UB, CD4002UB, CD4025UB Types

COS/MOS NOR Gates

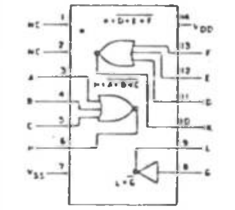
High-Voltage Types (20-Volt Rating)
Dual 3 Input
plus Inverter–CD4000UB
Quad 2 Input-CD4001UB
Dual 4 Input–CD4002UB
Triple 3 Input–CD4025UB

RCA-CD4000UB, CD4001UB, CD4002UB, and CD4025UB NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of COS/MOS gates.

The CD4000UB, CD4001UB, CD4002UB, and CD4025UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

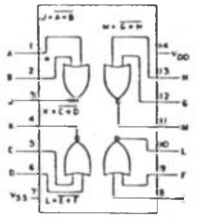
Features:

- Propagation delay time = 30 ns (typ.) at C_L = 50 pF, V_{DD} = 10 V
- Standardized symmetrical output characteristics
- 100% tested for maximum quiescent current at 20 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings



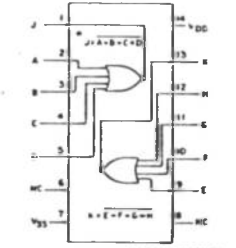
92CS 24757

CD4000UB
FUNCTIONAL DIAGRAM



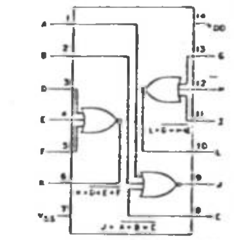
92CS 24762

CD4001UB
FUNCTIONAL DIAGRAM



92CS 24758

CD4002UB
FUNCTIONAL DIAGRAM



92CS 24760

CD4025UB
FUNCTIONAL DIAGRAM

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER-ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D, F, H Packages Values at –40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	µA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1				–	–	1	V
	1, 9	–	10	2				–	–	2	
	1.5,13.5	–	15	2.5				–	–	2.5	
Input High Voltage, V_{IH} Min.	0.5	–	5	4				4	–	–	
	1	–	10	8				8	–	–	
	1.5	–	15	12.5				12.5	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	µA

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

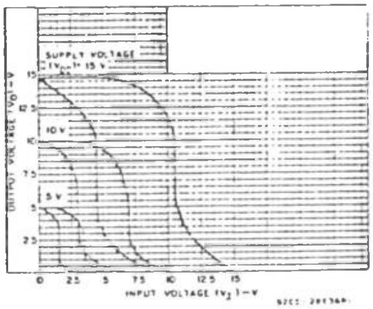


Fig. 1 – Minimum and maximum voltage transfer characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

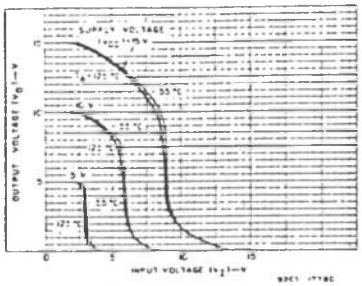


Fig. 2 – Typical voltage transfer characteristics as a function of temperature.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, and C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} Volts	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	60	120	ns
		10	30	60	
		15	25	50	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		10	15	pF

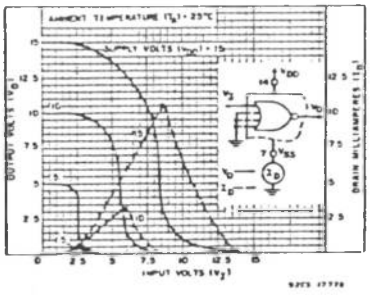


Fig. 3 – Typical current & voltage transfer characteristics.

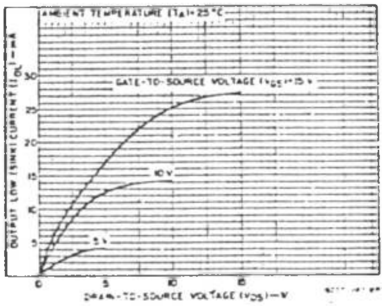


Fig. 5 – Typical output low (sink) current characteristics.

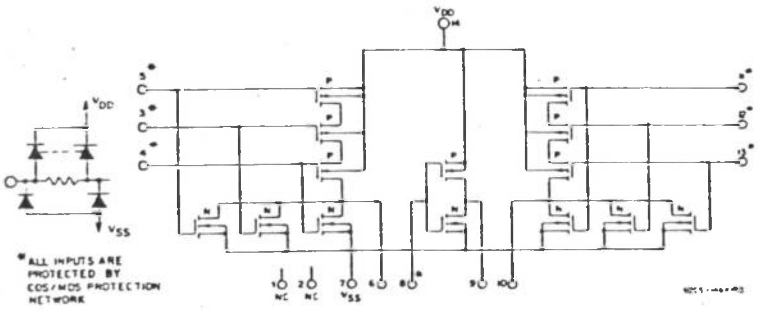
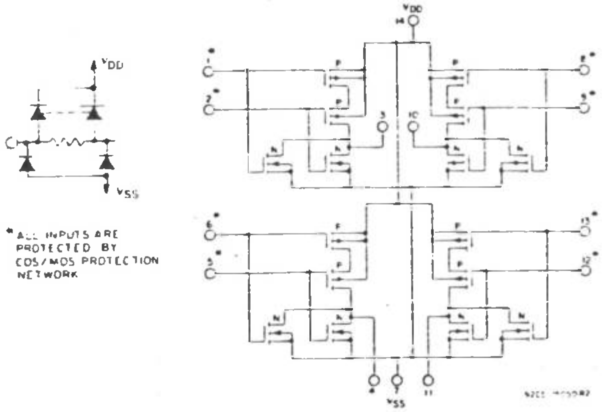
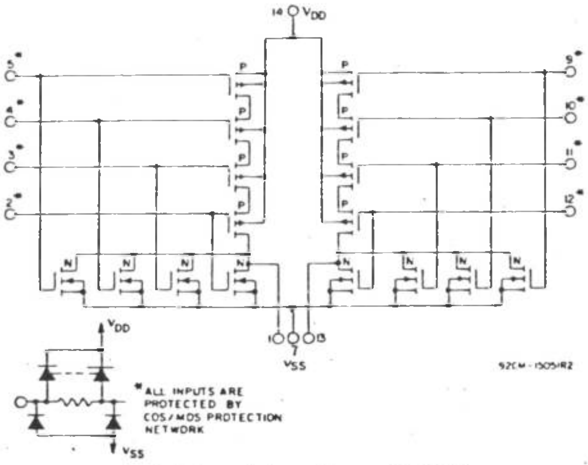


Fig. 4 – Schematic diagram for type CD4000UB.



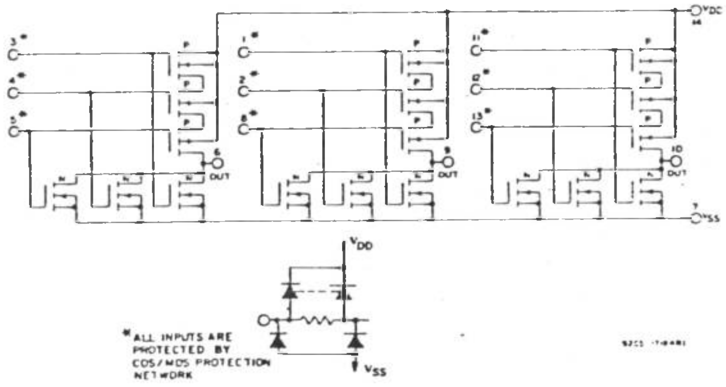
*ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

Fig. 6 – Schematic diagram for type CD4001UB.



*ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

Fig. 7 – Schematic diagram for type CD4002UB.



*ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

Fig. 8 – Schematic diagram for type CD4025UB.

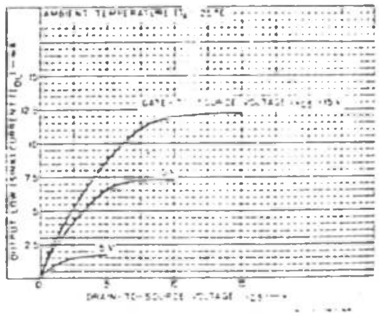


Fig 9 – Minimum output low (sink) current characteristics

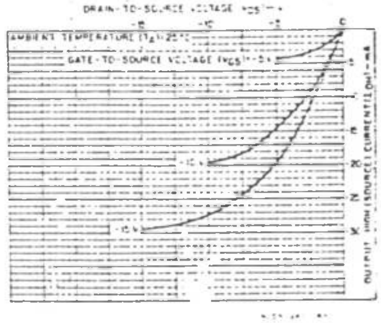


Fig. 10 – Typical output high (source) current characteristics

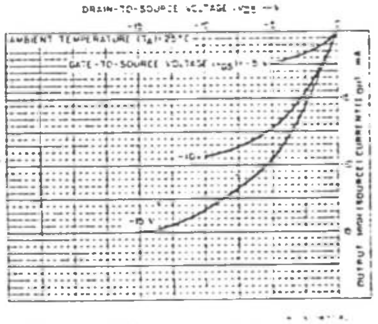


Fig 11 – Minimum output high (source) current characteristics

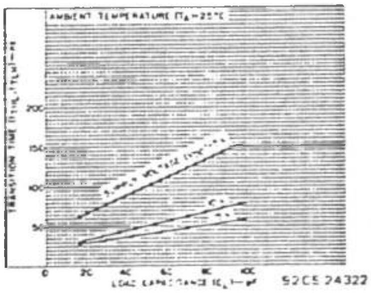


Fig 12 – Typical transition time vs. load capacitance.

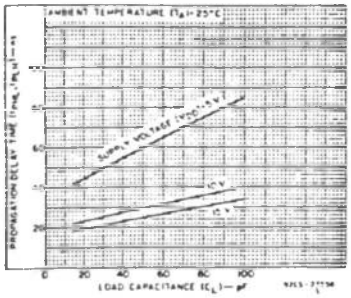


Fig. 13 – Typical propagation delay time vs. load capacitance.

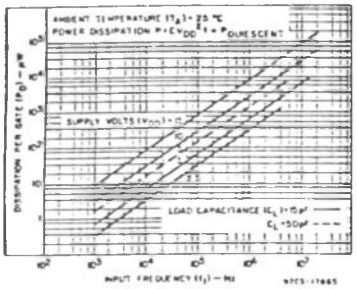


Fig. 14 – Typical power dissipation vs. frequency.

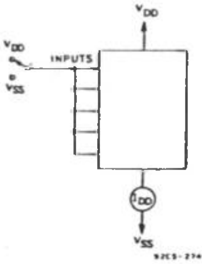


Fig. 15 – Quiescent-device-current test circuit.

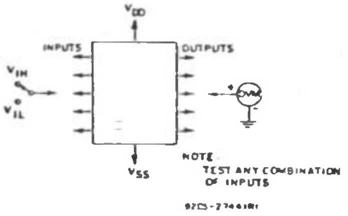


Fig. 16 – Input-voltage test circuit.

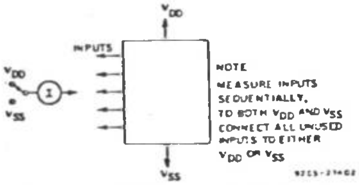
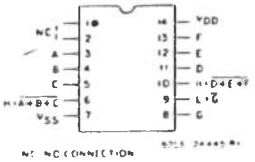
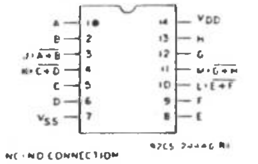

V_DD
INPUTS
V_DD
I
V_SS
V_SS
NOTE
MEASURE INPUTS SEQUENTIALLY, TO BOTH V_DD AND V_SS
CONNECT ALL UNUSED INPUTS TO EITHER V_DD OR V_SS
92CS-27402

Fig. 17 – Input leakage current test circuit.

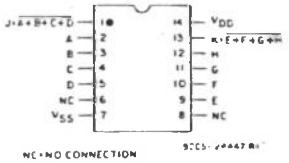
TERMINAL ASSIGNMENTS



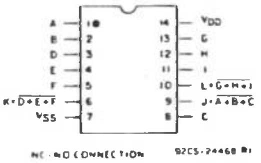
CD4000UB



CD4001UB



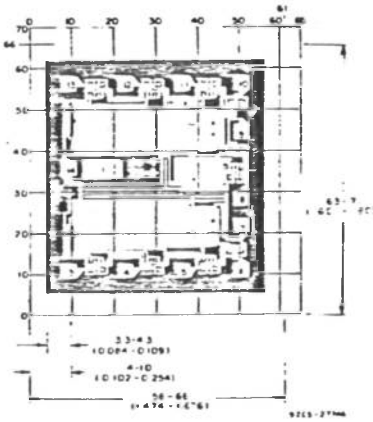
CD4002UB



CD4025UB

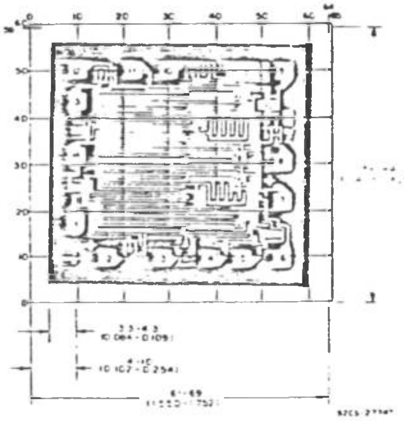
CHIP PHOTOGRAPHS

Dimensions and Pad Layouts

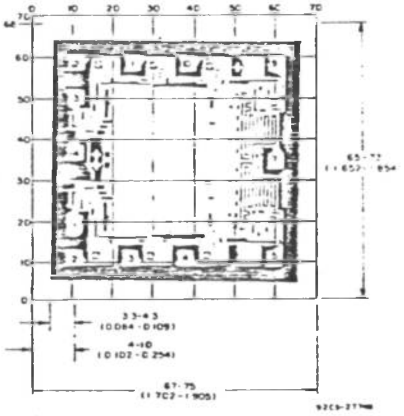


CD4000UB

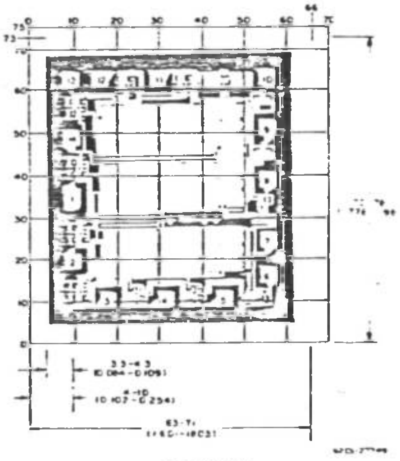
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).



CD4001UB



CD4002UB



CD4025UB

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS Dual 4-Stage Static Shift Register

With Serial Input/Parallel Output

High-Voltage Types (20-Volt Rating)

The RCA-CD4015B consists of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent CLOCK and RESET inputs as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the DATA input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one CD4015B package, or to more than 8 stages using additional CD4015B's is possible.

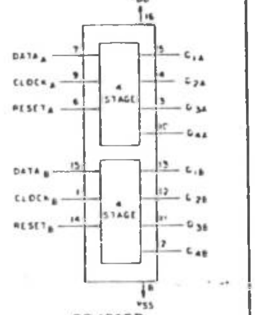
The CD4015B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).

Features:

- Medium speed operation . . . .
  12 MHz (typ.) clock rate at $V_{DD} - V_{SS} = 10$ V
- Fully static operation
- 8 master-slave flip-flops plus input and output buffering
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package-temperature range;
  100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
  1 V at $V_{DD} = 5$ V
  2 V at $V_{DD} = 10$ V
  2.5 V at $V_{DD} = 15$ V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

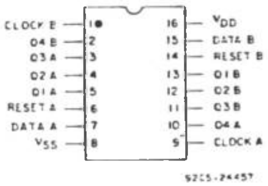
Applications:

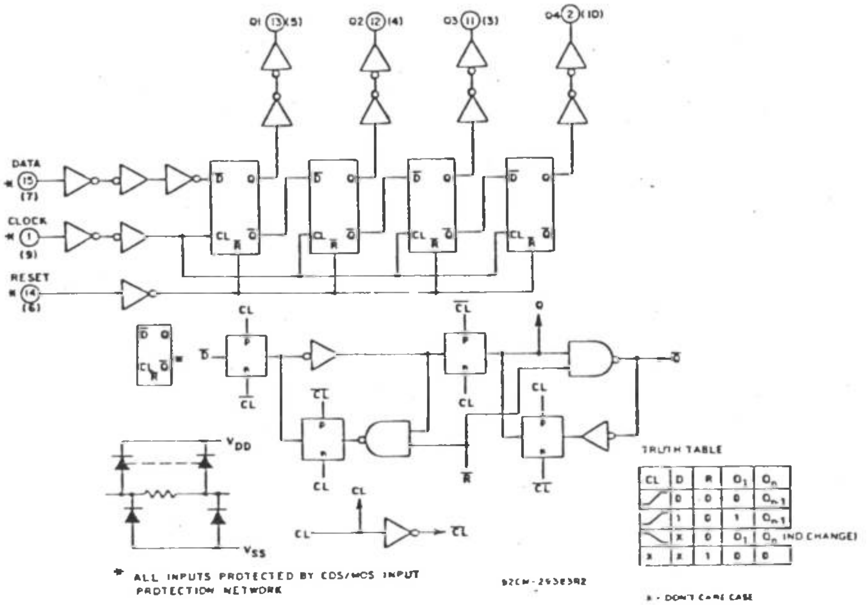
- Serial-input/parallel-output data queueing
- Serial to parallel data conversion
- General-purpose register



CD4015B
FUNCTIONAL DIAGRAM

TERMINAL DIAGRAM





TRUTH TABLE

CL	D	R	Q1	Qn
⟋	0	0	0	Q_{n-1}
⟋	1	0	1	Q_{n-1}
⟍	X	0	Q_1	Q_n (NO CHANGE)
X	X	1	0	0

X = DON'T CARE CASE

* ALL INPUTS PROTECTED BY COS/MOS INPUT PROTECTION NETWORK

Fig. 1 – Logic diagram (1 register).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		V_{DD} (V)	LIMITS		UNITS
			Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)			3	18	V
Clock Pulse Width,	t_WCL	5	180	–	ns
		10	80	–	
		15	50	–	
Clock Rise and Fall Time,	t_rCL, t_fCL	5	–		µs
		10	–	15	
		15	–		
Clock Input Frequency,	f_{CL}	5		3	MHz
		10	DC	6	
		15		8.5	
Data Setup Time,	t_{SU}	5	70	–	ns
		10	40	–	
		15	30	–	
Reset Pulse Width,	t_WR	5	200	–	
		10	80	–	
		15	60	–	

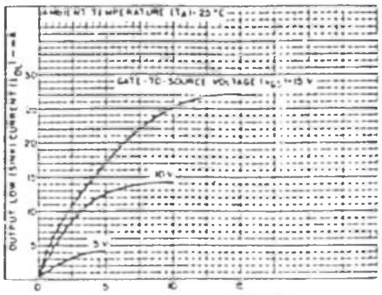


Fig. 2 – Typical output low (sink) current characteristics.

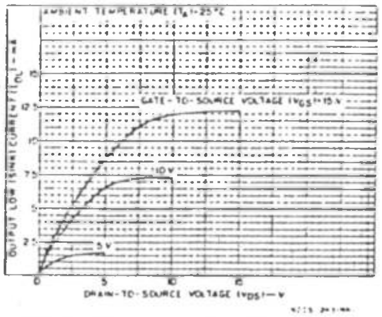


Fig. 3 – Minimum output low (sink) current characteristics.

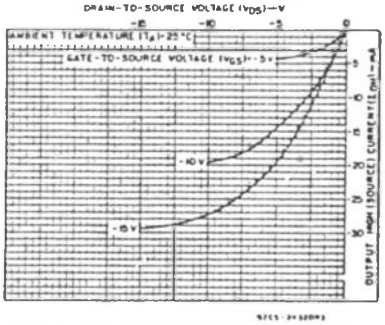


Fig. 4 – Typical output high (source) current characteristics.

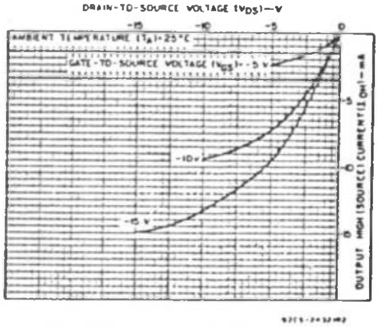


Fig. 5 – Minimum output high (source) current characteristics.

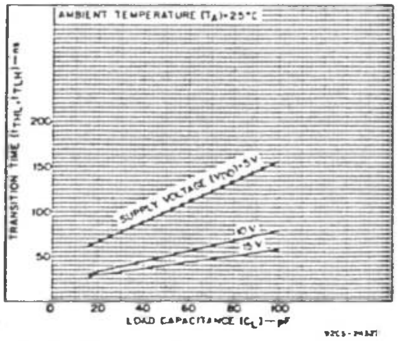


Fig. 6 – Typical transition time as a function of load capacitance.

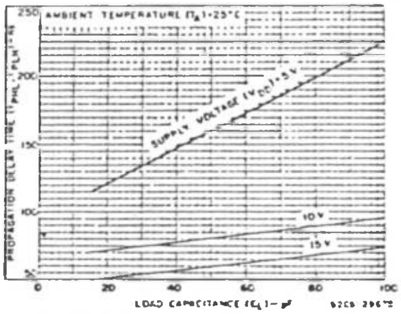
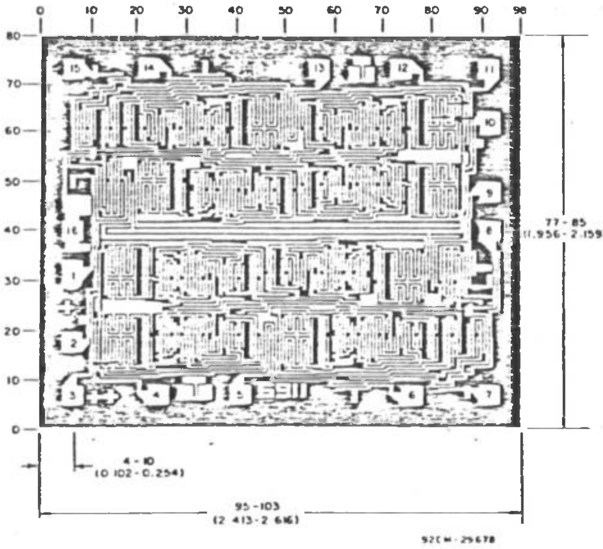


Fig 7 – Typical propagation delay time as a function of load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,K,F,H Packages Values at –40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)					+25			
				–55	–40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA



Photograph of Chip Layout for CD4015B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

DYNAMIC ELECTRICAL CHARACTERISTICS *at* $T_A = 25°C$*, Input* t_r*,* $t_f = 20\ ns$*,* $C_L = 50\ pF$*,* $R_L = 200\ k\Omega$

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
		V_{DD}(V)	Min.	Typ.	Max.	
CLOCKED OPERATION						
Propagation Delay Time; t_{PHL}, t_{PLH}		5	–	160	320	ns
		10	–	80	160	
		15	–	60	120	
Transition Time; t_{THL}, t_{TLH}		5	–	100	200	
		10	–	50	100	
		15	–	40	80	
Minimum Clock Pulse Width, t_WCL		5	–	90	180	
		10	–	40	80	
		15	–	25	50	
Clock Rise & Fall Time; t_rCL, t_fCL*		5	–	–	15	μs
		10	–	–	15	
		15	–	–	15	
Minimum Data Setup Time, t_{SU}		5	–	35	70	ns
		10	–	20	40	
		15	–	15	30	
Maximum Clock Input Frequency, f_{CL}		5	3	6	–	MHz
		10	6	12	–	
		15	8.5	17	–	
Input Capacitance, C_{IN}	Any Input		–	5	7.5	pF
RESET OPERATION						
Propagation Delay Time, t_{PHL},		5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
Minimum Reset Pulse Width t_WR		5	–	100	200	
		10	–	40	80	
		15	–	30	60	

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

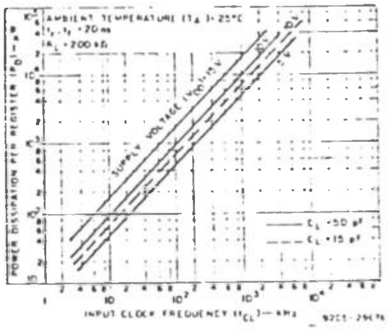


Fig. 8 – Typical power dissipation as a function of frequency.

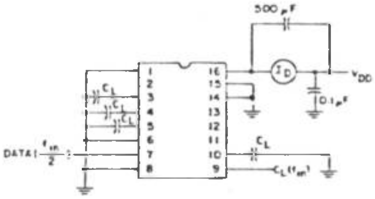


Fig. 9 – Power dissipation test circuit.

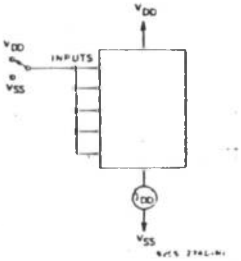


Fig. 10 – Quiescent device current test circuit.

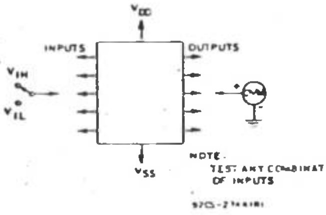


Fig. 11 – Input voltage test circuit.

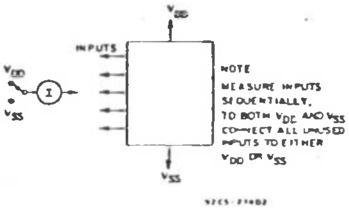

V_{DD}
INPUTS
V_{DD}
I
V_{SS}
V_{SS}
NOTE
MEASURE INPUTS SEQUENTIALLY,
TO BOTH V_{DD} AND V_{SS}
CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}
92CS-27402

Fig. 12 – Input current test circuit.

COS/MOS
Hex Buffer/Converters

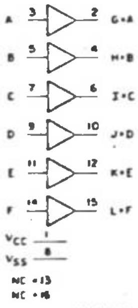
High-Voltage Types (20-Volt Rating)

CD4049UB–Inverting Type
CD4050B–Non-Inverting Type

The RCA-CD4049UB and CD4050B are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as COS/MOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC}=5 V, $V_{OL} \leq 0.4$ V, and $I_{OL} \geq 3.2$ mA.)

The CD4049UB and CD4050B are designated as replacements for CD4009UB and CD4010B, respectively. Because the CD4049UB and CD4050B require only one power supply, they are preferred over the CD4009UB and CD4010B and should be used in place of the CD4009UB and CD4010B in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049UB and CD4050B are pin compatible with the CD4009UB and CD4010B respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049UB or CD4050B, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink-current or voltage conversion, the CD4069UB Hex Inverter is recommended.

The CD4049UB and CD4050B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).



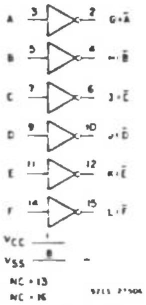
CD4050B
FUNCTIONAL DIAGRAM

Features:

- High sink current for driving 2 TTL loads
- High-to-low level logic conversion
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-, 10-, and 15-volt parametric ratings

Applications:

- COS/MOS to DTL/TTL hex converter
- COS/MOS current "sink" or "source" driver
- COS/MOS high-to-low logic-level converter



CD4049UB
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC})	
(Voltages referenced to V_{SS} Terminal)	–0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5 to +20.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = –40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D, F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	–55 to +125°C
PACKAGE TYPE E	–40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	–65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (V_{CC}) (For T_A=Full Package-Temperature Range)	3	18	V
Input Voltage Range (V_{IN})	V_{CC}*	18	V

*The CD4049 and CD4050 have high-to-low-level voltage conversion capability but not low-to-high-level; therefore it is recommended that $V_{IN} \geq V_{CC}$.

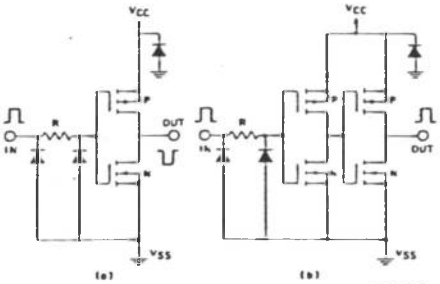


Fig. 1–a) Schematic diagram of CD4049UB, 1 of 6 identical units;
b) Schematic diagram of CD4050B, 1 of 6 identical units.

CD4049UB, CD4050B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARAC-TERISTIC	CONDITIONS			Limits At Indicated Temperatures (°C) *Values at −55,+25,+125 Apply to D,F,H Pkgs. Values at −40,+25,+85 Apply to E Package*							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	4.5	3.3	3.1	2.1	1.8	2.6	5.2	–	mA
	0.4	0,5	5	4	3.8	2.9	2.4	3.2	6.4	–	
	0.5	0,10	10	10	9.6	6.6	5.6	8	16	–	
	1.5	0,15	15	26	25	20	18	24	48	–	
Output High (Source) Current I_{OH} Min.	4.6	0,5	5	−1	−0.9	−0.72	−0.6	−0.8	−1.6	–	
	2.5	0,5	5	−4	−3.6	−2.6	−2.3	−3.2	−6.4	–	
	9.5	0,10	10	−2.2	−2	−1.5	−1.3	−1.8	−3.6	–	
	13.5	0,15	15	−6.6	−6.4	−5	−4.4	−6	−12	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05					0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage: V_{IL} Max. CD4049UB	4.5	–	5	1				–	–	1	V
	9	–	10	2				–	–	2	
	13.5	–	15	2.5				–	–	2.5	
Input Low Voltage: V_{IL} Max. CD4050B	0.5	–	5	1.5				–	–	1.5	
	1	–	10	3				–	–	3	
	1.5	–	15	4				–	–	4	
Input High Voltage: V_{IH} Min. CD4049UB	0.5	–	5	4				4	–	–	
	1	–	10	8				8	–	–	
	1.5	–	15	12.5				12.5	–	–	
Input High Voltage: V_{IH} Min. CD4050B	4.5	–	5	3.5				3.5	–	–	
	9	–	10	7				7	–	–	
	13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

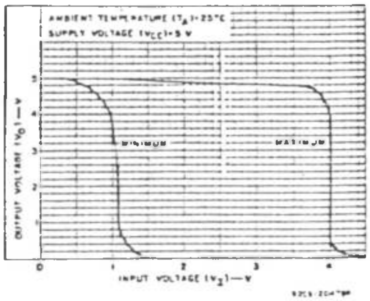


Fig. 2—Minimum and maximum voltage transfer characteristics for CD4049UB.

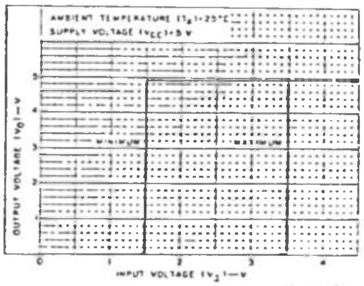


Fig. 3—Minimum and maximum voltage transfer characteristics for CD4050B.

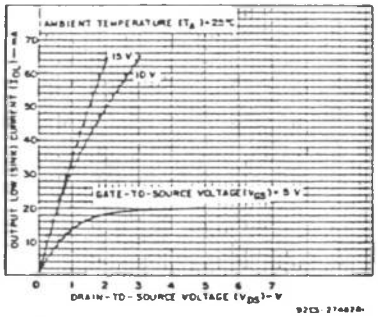


Fig. 4 — Typical output low (sink) current characteristics.

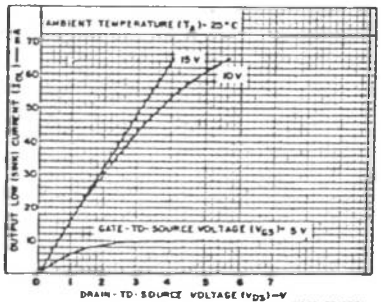


Fig. 5 — Minimum output low (sink) current drain characteristics.

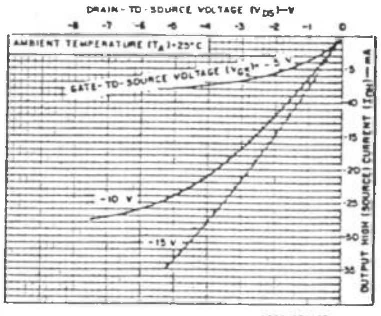


Fig. 6 — Typical output high (source) current characteristics.

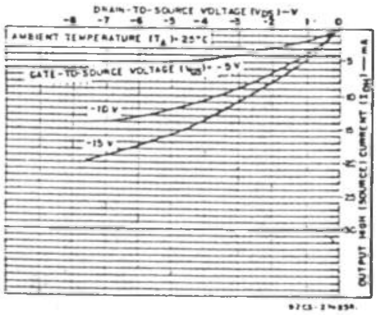


Fig. 7 — Minimum output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; Input t_r,t_f=20 ns, C_L=50 pF, R_L=200 kΩ

CHARACTERISTIC	CONDITIONS		LIMITS ALL PKGS.		UNITS
	V_{IN}	V_{CC}	Typ.	Max.	
Propagation Delay Time: Low-to-High, t_{PLH} CD4049UB	5	5	60	120	ns
	10	10	32	65	
	10	5	45	90	
	15	15	25	50	
	15	5	45	90	
CD4050B	5	5	70	140	
	10	10	40	80	
	10	5	45	90	
	15	15	30	60	
	15	5	40	80	
High-to-Low, t_{PHL} CD4049UB	5	5	32	65	ns
	10	10	20	40	
	10	5	15	30	
	15	15	15	30	
	15	5	10	20	
CD4050B	5	5	55	110	
	10	10	22	55	
	10	5	50	100	
	15	15	15	30	
	15	5	50	100	
Transition Time: Low-to-High, t_{TLH}	5	5	80	160	ns
	10	10	40	80	
	15	15	30	60	
High-to-Low, t_{THL}	5	5	30	60	
	10	10	20	40	
	15	15	15	30	
Input Capacitance, C_{IN} CD4049UB	–	–	15	22.5	pF
CD4050B	–	–	5	7.5	

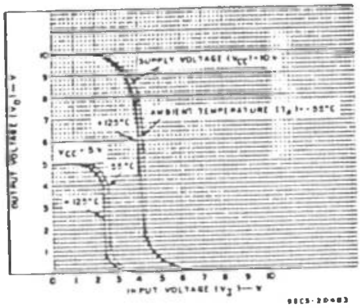


Fig. 8 – Typical voltage transfer characteristics as a function of temperature for CD4049UB.

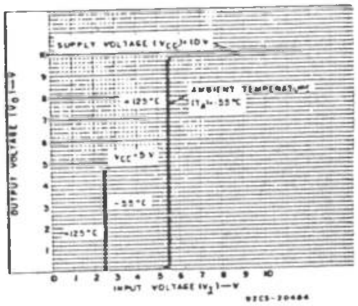


Fig. 9 – Typical voltage transfer characteristics as a function of temperature for CD4050B.

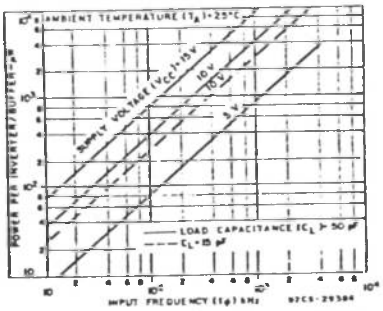


Fig. 10 – Typical power dissipation vs. frequency characteristics.

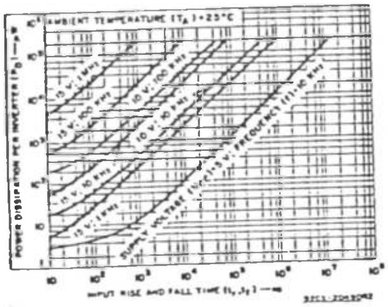


Fig. 11 – Typical power dissipation vs. input rise and fall times per inverter for CD4049UB.

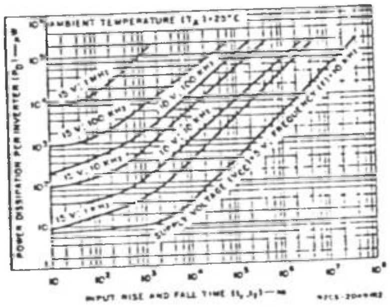


Fig. 12 – Typical power dissipation vs. input rise and fall times per inverter for CD4050B.

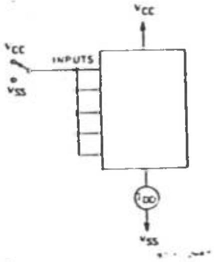


Fig. 13 – Quiescent device current test circuit.

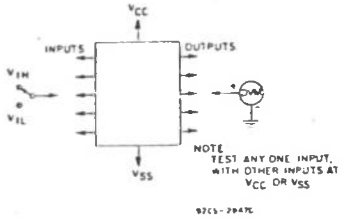


Fig. 14 – Input voltage test circuit.

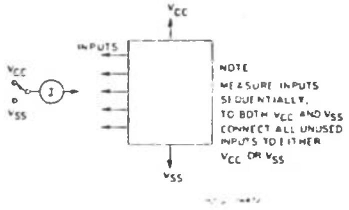

VCC
INPUTS
VCC
VSS
I
VSS
NOTE
MEASURE INPUTS SEQUENTIALLY, TO BOTH VCC AND VSS
CONNECT ALL UNUSED INPUTS TO EITHER VCC OR VSS

Fig. 15 – Input current test circuit.

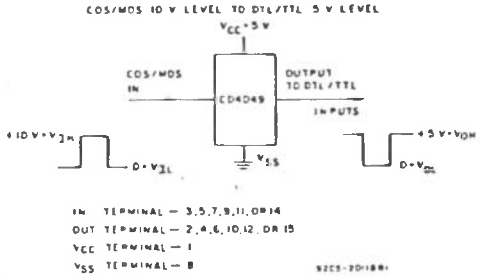
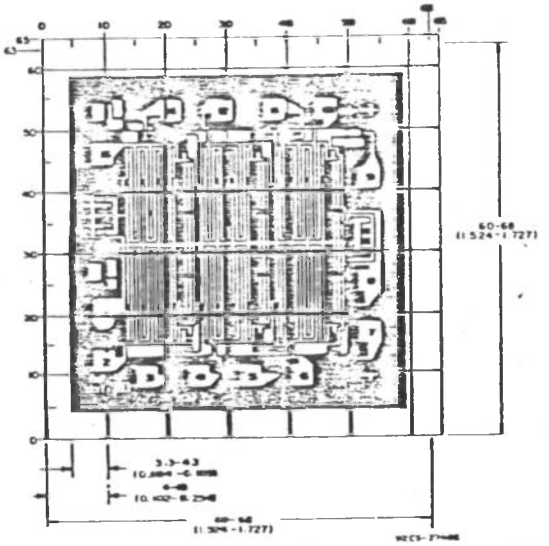


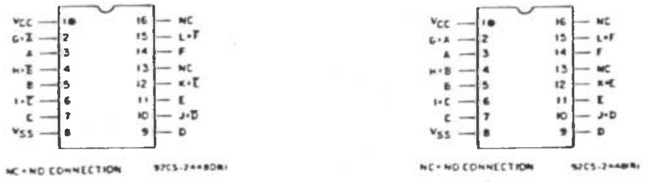
Fig. 16 – Logic-level conversion application.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Photograph of chip for CD4049UB. Dimensions and pad layout for CD4050B are identical.

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.



CD4049

CD4050

TERMINAL ASSIGNMENTS

Preliminary Data

COS/MOS 14-Stage Ripple-Carry Binary Counter/Divider and Oscillator

High-Voltage Types (20-Volt Rating)

The RCA-CD4060B consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which resets the counter to the all-O's state and disables the oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of ϕ_1 (and ϕ_0). All inputs and outputs are fully buffered. Schmitt trigger action on the input-pulse line permits unlimited input-pulse rise and fall times.

The CD4060B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

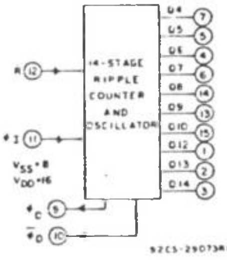
Features:

- Medium-speed operation
- Common reset
- Fully static operation
- Buffered inputs and outputs
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for description of "B" Series CMOS Devices"

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V



FUNCTIONAL DIAGRAM

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D, F, H Packages Values at –40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current* I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current,* I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5, 13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5, 13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

*Data not applicable to terminal 9 or 10.

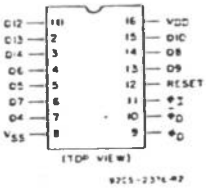
Oscillator Features:

- All active components on chip
- RC or crystal oscillator configuration

Applications

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits

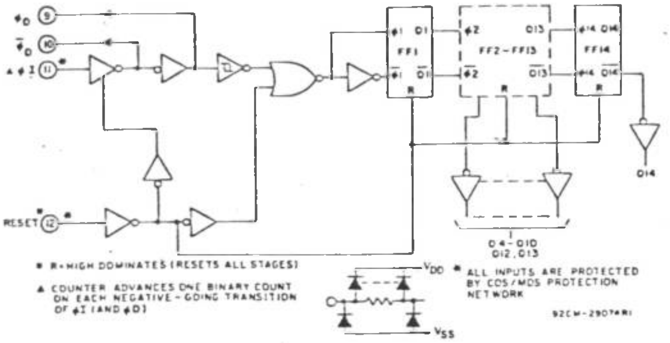
TERMINAL DIAGRAM



CD4060B Types

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D)	
For T_A = 40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING TEMPERATURE RANGE (T_A)	
PACKAGE TYPES D, F, H	55 to +125°C
PACKAGE TYPE E	40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max	+265°C



ϕ_O 9
$\bar{\phi}_O$ 10
▲ϕI 11
FF1
FF2–FF13
FF14
ϕ1 Q1
ϕ2 Q13
ϕ14 Q14
R
Q14
Q4–Q10
Q12, Q13
RESET 12
■ R-HIGH DOMINATES (RESETS ALL STAGES)
▲ COUNTER ADVANCES ONE BINARY COUNT ON EACH NEGATIVE-GOING TRANSITION OF ϕI (AND ϕO)
VDD
VSS
★ ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK
92CM-29074R1

Fig.1 – Logic diagram.

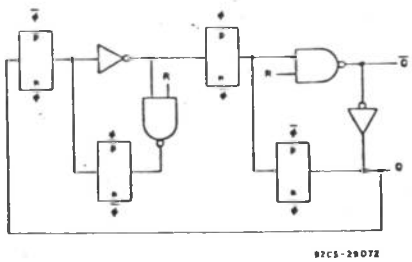


Fig.2 – Detail of typical flip-flop stage.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES	UNITS
		V_{DD} (V)		
Input-Pulse Operation				
Propagation Delay Time, ϕ_1 to Q4 Out; t_{PHL}, t_{PLH}		5	800	ns
		10	340	
		15	240	
Propagation Delay Time, Q_n to Q_{n+1}; t_{PHL}, t_{PLH}		5	200	ns
		10	85	
		15	60	
Transition Time, t_{THL}, t_{TLH}		5	100	ns
		10	50	
		15	40	
Min. Input-Pulse Width, t_W	f = 100 kHz	5	70	ns
		10	30	
		15	20	
Input-Pulse Rise & Fall Time, $t_{r\phi}$, $t_{f\phi}$		5	Unlimited	μs
		10		
		15		
Max. Input-Pulse Frequency, f_ϕ		5	7	MHz
		10	16	
		15	24	
Input Capacitance, C_I	Any Input		5	pF
Reset Operation				
Propagation Delay Time, t_{PHL}		5	300	ns
		10	140	
		15	100	
Minimum Reset Pulse Width, t_W		5	375	ns
		10	200	
		15	150	

COS/MOS 4-Bit Magnitude Comparator

High Voltage Types (20-Volt Rating)

The RCA-CD4063B is a 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to", or "greater than" a second 4-bit word.

The CD4063B has eight comparing inputs (A3, B3, through A0, B0), three outputs (A < B, A = B, A > B) and three cascading inputs (A < B, A = B, A > B) that permit systems designers to expand the comparator function to 8, 12, 16 . . . 4N bits. When a single CD4063B is used, the cascading inputs are connected as follows: (A < B) = low, (A = B) = high, (A > B) = low.

For words longer than 4 bits, CD4063B devices may be cascaded by connecting the outputs of the less-significant comparator to the corresponding cascading inputs of the more-significant comparator. Cascading inputs (A < B, A = B, and A > B) on the least significant comparator are connected to a low, a high, and a low level, respectively.

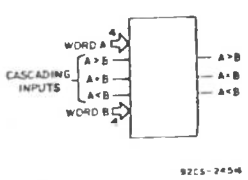
The CD4063B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix). This device is pin-compatible with the standard 7485 TTL type.

Features:

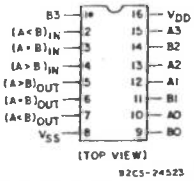
- Expansion to 8, 12, 16....4N bits by cascading units
- Medium-speed operation:
  compares two 4-bit words
  in 250 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Standardized symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V
  over full package temperature range;
  100 nA at 18 V and 25°C
- Noise margin (full package temperature range)
  range) = 1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Servo motor controls
- Process controllers



FUNCTIONAL DIAGRAM



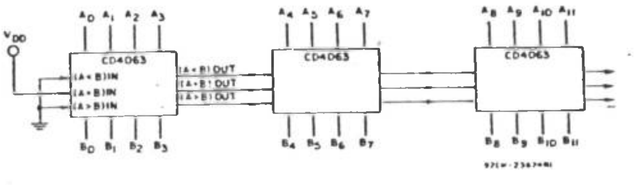
TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V



t_p TOTAL = t_p (COMPARE INPUTS) + 2 × t_p (CASCADE INPUTS), AT V_{DD} = 10V
(3 STAGES)
= 250 + (2 × 200) = 650 ns (TYP.)

Fig. 1 — Typical speed characteristics of a 12-bit comparator.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A < B	A = B	A > B	A < B	A = B	A > B
A3 > B3	X	X	X	X	X	X	0	0	1
A3 = B3	A2 > B2	X	X	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	0	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	0	1	0	0
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	1	0	0
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	1	0	0
A3 = B3	A2 < B2	X	X	X	X	X	1	0	0
A3 < B3	X	X	X	X	X	X	1	0	0

X = Don't Care   Logic 1 ≡ High Level   Logic 0 ≡ Low Level

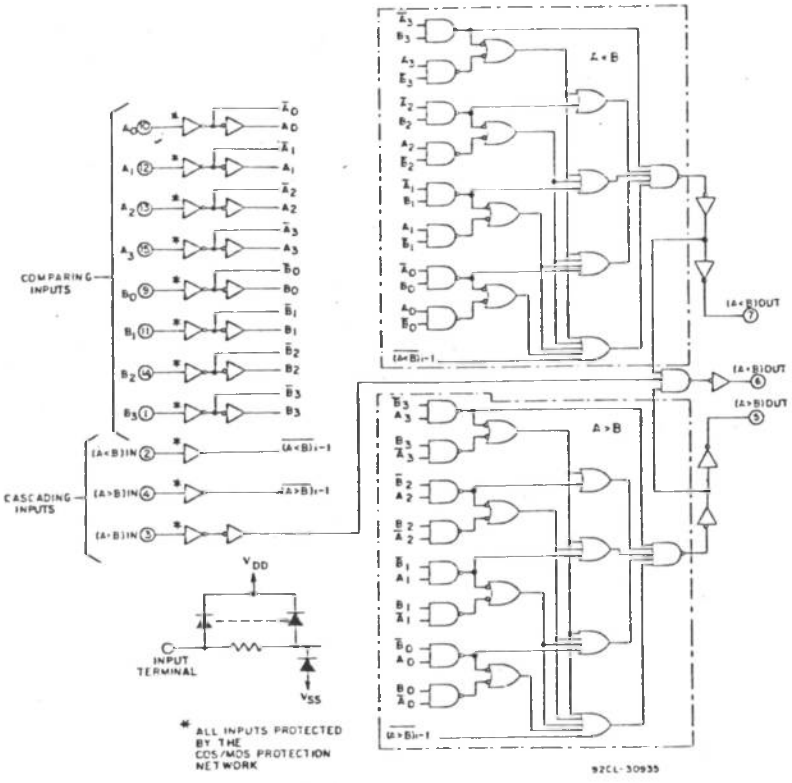


Fig. 2 — Logic diagram for CD4063B.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ C$; Input t_r, $t_f = 20\ ns$, $C_L = 50\ pF$, $R_L = 200k\Omega$

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} Volts	Typ.	Max.	
Propagation Delay Time: Comparing Inputs to Outputs, t_{PHL}, t_{PLH}		5	625	1250	ns
		10	250	500	
		15	175	350	
Cascading Inputs to Outputs, t_{PHL}, t_{PLH}		5	500	1000	
		10	200	400	
		15	140	280	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

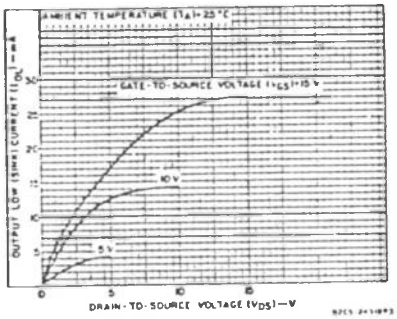


Fig. 3 — Typical output low (sink) current characteristics.

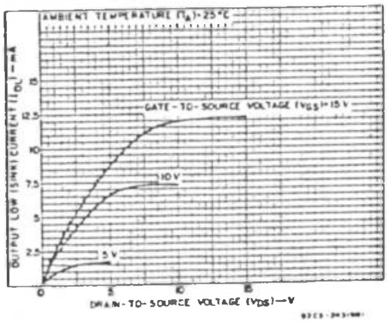


Fig. 4 — Minimum output low (sink) current characteristics.

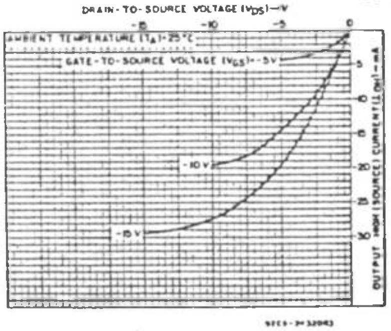


Fig. 5 — Typical output high (source) current characteristics.

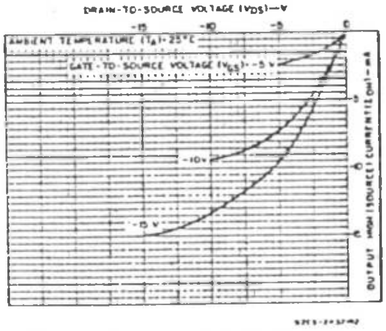


Fig. 6 — Minimum output high (source) current characteristics.

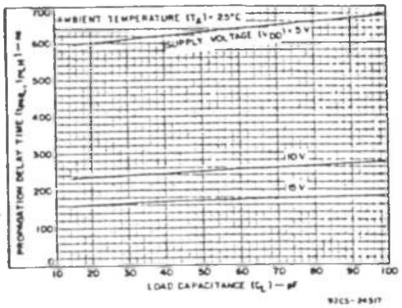


Fig. 7 — Typical propagation delay time vs. load capacitance ("comparing inputs" to outputs).

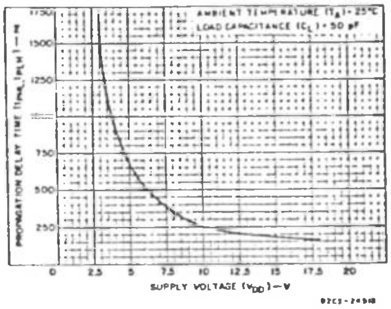


Fig. 8 — Typical propagation delay time vs. supply voltage ("comparing inputs" to outputs).

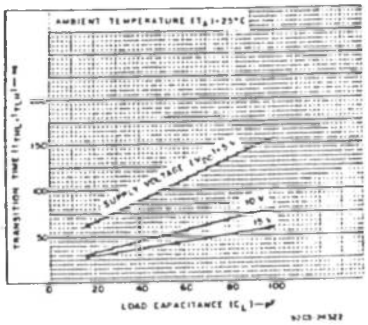


Fig. 9 — Typical transition time vs. load capacitance.

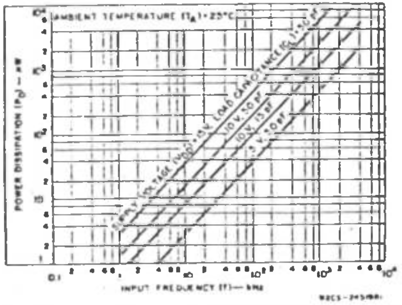


Fig. 10 — Typical power dissipation vs. frequency (see Fig. 12 — dynamic power dissipation test circuit).

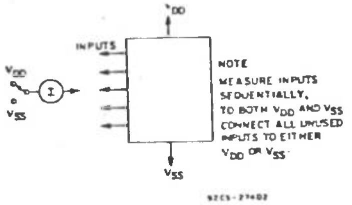

V_DD
INPUTS
V_DD
V_SS
V_SS
NOTE
MEASURE INPUTS SEQUENTIALLY, TO BOTH V_DD AND V_SS CONNECT ALL UNUSED INPUTS TO EITHER V_DD OR V_SS.
92CS-27402

Fig. 11 — Input current test circuit.

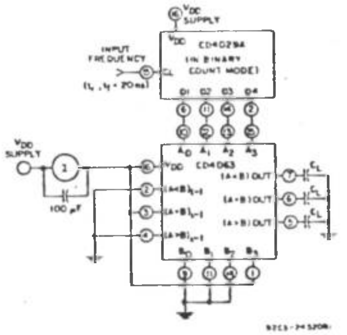


Fig. 12 — Dynamic power dissipation test circuit

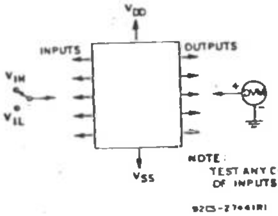


Fig. 13 — Input-voltage test circuit.

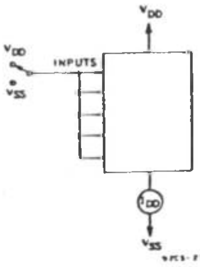
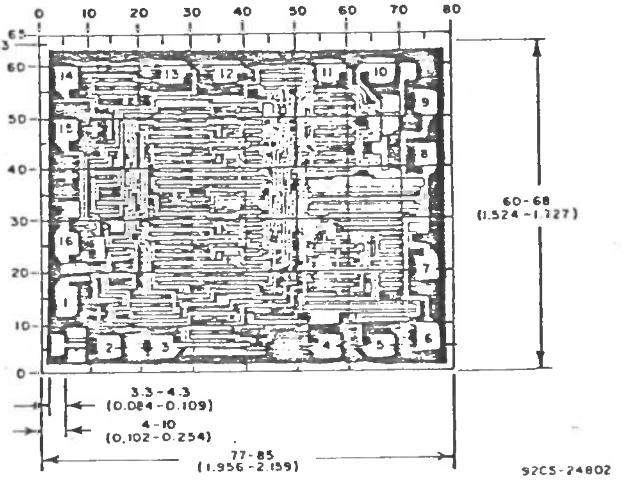


Fig. 14 — Quiescent-device-current test circuit.



Dimensions and pad layout for CD4063BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4066B Types

COS/MOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

High-Voltage Types (20-Volt Rating)

The RCA-CD4066B is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with RCA-CD4016B, but exhibits a much lower on-state resistance. In addition, the on-state resistance is relatively constant over the full input-signal range.

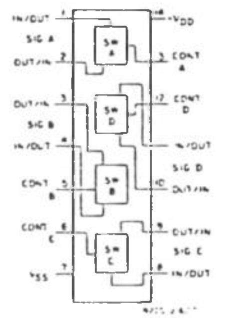
The CD4066B consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased on or off simultaneously by the control signal. As shown in Fig.1, the well of the n-channel device on each switch is either tied to the input when the switch is on or to V_{SS} when the switch is off. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the on-state resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant on-state impedance over the input-signal range. For sample-and-hold applications, however, the CD4016B is recommended.

The CD4066B is available in 14-lead ceramic dual-in-line packages (D and F suffixes), 14-lead plastic dual-in-line packages (E suffix), and in chip form (H suffix).

Features:

- 15-V digital or ±7.5-V peak-to-peak switching
- 125Ω typical on-state resistance for 15-V operation
- Switch on-state resistance matched to within 5 Ω over 15-V signal-input range
- On-state resistance flat over full peak-to-peak signal range
- High on/off output-voltage ratio: 80 dB typ. @ f_{is} = 10 kHz, R_L = 1 kΩ
- High degree of linearity: <0.5% distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 Vp-p, $V_{DD} - V_{SS} \geqslant 10$ V, R_L = 10 kΩ
- Extremely low off-state switch leakage resulting in very low offset current and high effective off-state resistance: 10 pA typ. @ $V_{DD} - V_{SS}$ = 10 V, T_A = 25°C
- Extremely high control input impedance (control circuit isolated from signal circuit): 10^{12} Ω typ.
- Low crosstalk between switches: −50 dB typ. @ f_{is} = 8 MHz, R_L = 1 kΩ
- Matched control-input to signal-output capacitance: Reduces output signal transients
- Frequency response, switch on = 40 MHz (typ.)
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of "B" Series CMOS Devices"



FUNCTIONAL DIAGRAM

Applications:

- Analog signal switching/multiplexing
  - Signal gating
  - Modulator
  - Squelch control
  - Demodulator
  - Chopper
  - Commutating switch
- Digital signal switching/Multiplexing
- Transmission-gate logic implementation
- Analog-to-digital & digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

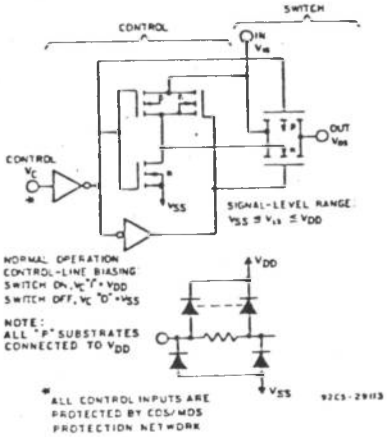


Fig. 1 – Schematic diagram of 1 of 4 identical switches and its associated control circuitry.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

ELECTRICAL CHARACTERISTICS

Characteristic	Test Conditions			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages Values at −40, +25, +85 Apply to E Package						UNITS
		V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD}	–	0,5	5	0.25	0.25	7.5	7.5	0.01	0.25	μA
		0,10	10	0.5	0.5	15	15	0.01	0.5	
		0,15	15	1	1	30	30	0.01	1	
		0,20	20	5	5	150	150	0.02	5	
Signal Inputs (V_{is}) and Output (V_{os})										
On-State Resistance, r_{on} Max.	$V_C = V_{DD}$ $R_L = 10\ k\Omega$ returned to $\frac{V_{DD} - V_{SS}}{2}$ $V_{is} = V_{SS}$ to V_{DD}		5	800	850	1200	1300	470	1050	Ω
			10	310	330	500	550	180	400	
			15	200	210	300	320	125	240	
Δ On-State Resistance Between Any 2 Switches, Δr_{on}	$R_L = 10\ k\Omega$, $V_C = V_{DD}$		5	–	–	–	–	15	–	Ω
			10	–	–	–	–	10	–	
			15	–	–	–	–	5	–	
Total Harmonic Distortion, THD	$V_C = V_{DD} = 5\ V$, $V_{SS} = -5\ V$, $V_{is(p\text{-}p)} = 5\ V$ (Sine wave centered on 0 V) $R_L = 10\ k\Omega$, $f_{is} = 1\ kHz$ sine wave			–	–	–	–	0.4	–	%
−3dB Cutoff Frequency (Switch on)	$V_C = V_{DD} = 5\ V$, $V_{SS} = -5\ V$, $V_{is(p\text{-}p)} = 5\ V$ (Sine wave centered on 0 V $R_L = 1\ k\Omega$,			–	–	–	–	40	–	MHz
−50dB Feed-through Frequency (Switch off)	$V_C = V_{SS} = -5\ V$, $V_{is(p\text{-}p)} = 5\ V$ Sine wave centerd on 0 V $R_L = 1\ k\Omega$			–	–	–	–	1	–	MHz
Input/Output Leakage Current (Switch off) I_{is} Max.	$V_C = 0\ V$ $V_{is} = 18\ V$; $V_{os} = 0\ V$, $V_{is} = 0 V$; $V_{os} = 18\ V$		18	±0.1	±0.1	±1	±1	$\pm 10^{-5}$	±0.1	μA
−50 dB Crosstalk Frequency	$V_C(A) = V_{DD} = +5\ V$, $V_C(B) = V_{SS} = -5\ V$, $V_{is}(A) = 5\ V_{p\text{-}p}$, 50 Ω source $R_L = 1\ k\Omega$			–	–	–	–	8	–	MHz
Propagation Delay (Signal Input to Signal Output) t_{pd}	$R_L = 200\ k\Omega$ $V_C = V_{DD}$, $V_{SS} = GND$, $C_L = 50\ pF$ $V_{is} = 10\ V$ (Square wave centered on 5 V t_r, $t_f = 20\ ns$		5	–	–	–	–	20	40	ns
			10	–	–	–	–	10	20	
			15	–	–	–	–	7	15	
Capacitance: Input, C_{is}	$V_{DD} = +5\ V$ $V_C = V_{SS} = -5\ V$			–	–	–	–	8	–	pF
Output, C_{os}				–	–	–	–	8	–	
Feedthrough, C_{ios}				–	–	–	–	0.5	–	

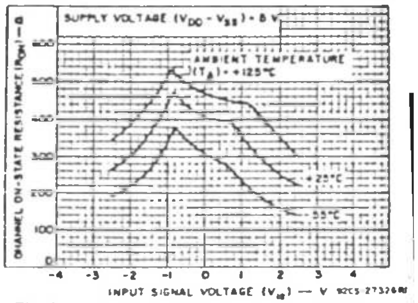


Fig. 2— Typical on-state resistance vs. input signal voltage (all types).

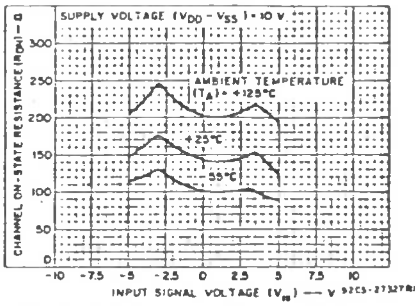


Fig. 3— Typical on-state vs. input signal voltage (all types).

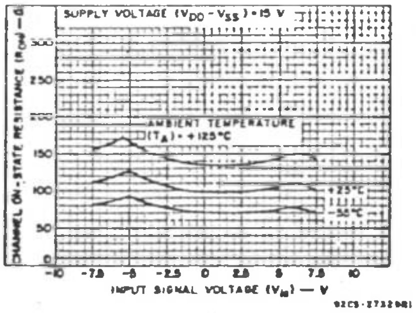


Fig. 4— Typical on-state resistance vs. input signal voltage (all types).

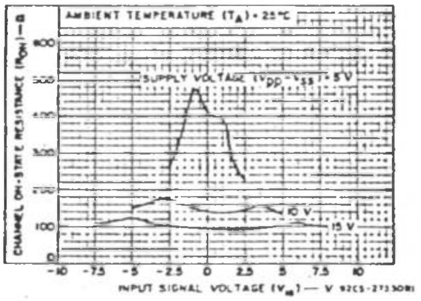


Fig. 5— on-state resistance vs. input signal voltage (all types).

ELECTRICAL CHARACTERISTICS (cont'd)

Characteristic	Test Conditions	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D, F, H Packages Values at –40, +25, +85 Apply to E Package						UNITS
			–55	–40	+85	+125	+25 Typ.	+25 Max.	
Control (V_C)									
Control Input Low Voltage, V_{ILC} Max.	$/I_{is}/ < 10\,\mu A$ $V_{is} = V_{SS}$, $V_{OS} = V_{DD}$ and $V_{is} = V_{DD}$, $V_{OS} = V_{SS}$	5	1	1	1	1	–	1	V
		10	2	2	2	2	–	2	
		15	2	2	2	2	–	2	
Control Input High Voltage, V_{IHC}	See Fig. 6	5	3.5 (Min.)						V
		10	7 (Min.)						
		15	11 (Min.)						
Input Current, I_{IN} Max.	$V_{is} \leq V_{DD}$ $V_{DD} - V_{SS} = 18\text{ V}$ $V_{CC} \leq V_{DD} - V_{SS}$	18	±0.1	±0.1	±1	±1	$\pm10^{-5}$	±0.1	µA
Crosstalk (Control Input to Signal Output)	$V_C = 10\text{ V}$ (Sq. Wave) $t_r, t_f = 20\text{ ns}$ $R_L = 10\text{ k}\Omega$	10	–	–	–	–	50	–	mV
Turn-On Propagation Delay	$V_{DD} - V_{SS} = 10\text{ V}$ $t_r, t_f = 20\text{ ns}$ $C_L = 50\text{ pF}$ $R_L = 1\text{ k}\Omega$	5	–	–	–	–	35	70	ns
		10	–	–	–	–	20	40	
		15	–	–	–	–	15	30	
Maximum Control Input Repetition Rate	$V_{is} = V_{DD}$, V_{SS} = GND, $R_L = 1\text{ k}\Omega$ to gnd, $C_L = 50\text{ pF}$, $V_C = 10\text{ V}$ (Square wave centered on 5 V) $t_r, t_f = 20\text{ ns}$, $V_{os} = ½\, V_{os}$ @ 1 kHz	5	–	–	–	–	6	–	MHz
		10	–	–	–	–	9	–	
		15	–	–	–	–	9.5	–	
Input Capacitance, C_{IN}			–	–	–	–	5	7.5	µF

V_{DD} (V)	V_{is} (V)	Switch Input I_{is} (mA)					Switch Output, V_{os} (V)	
		–55°C	–40°C	+25°C	+85°C	+125°C	Min.	Max.
5	0	0.64	0.61	0.51	0.42	0.36	–	0.4
5	5	–0.64	–0.61	–0.51	–0.42	–0.36	4.6	–
10	0	1.6	1.5	1.3	1.1	0.9	–	0.5
10	10	–1.6	–1.5	–1.3	–1.1	–0.9	9.5	–
15	0	4.2	4	3.4	2.8	2.4	–	1.5
15	15	–4.2	–4	–3.4	–2.8	–2.4	13.5	–

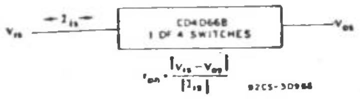


Fig. 6 – Determination of r_{on} as a test condition for control input high voltage (V_{IHC}) specification.

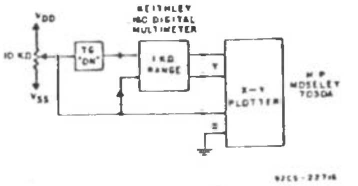


Fig. 7 – Channel on-state resistance measurement circuit.

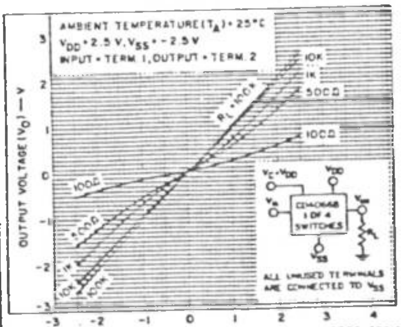


Fig. 8 – Typical r_{on} characteristics for 1 of 4 channels.

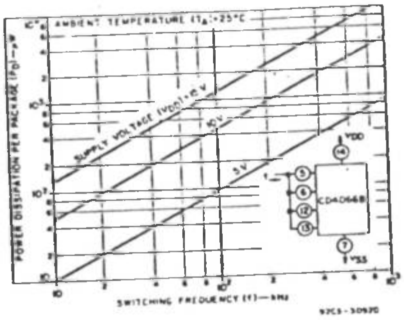


Fig. 9 – Power dissipation per package vs. switching frequency.

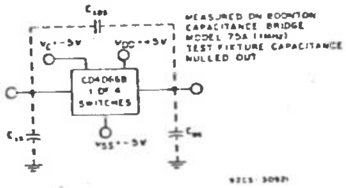


Fig. 10 – Capacitance test circuit.

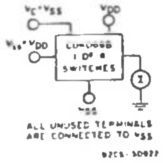


Fig. 11 – Off-switch input or output leakage.

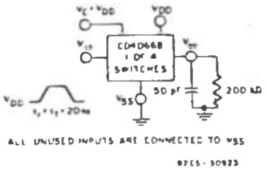


Fig. 12 – Propagation delay time signal input (V_{is}) to signal output (V_{os}).

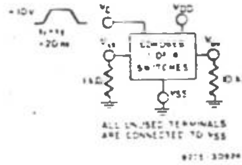


Fig. 13 – Crosstalk-control input to signal output.

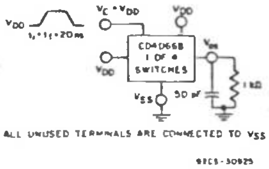


Fig. 14 – Propagation delay t_{PLH}, t_{PHL} control-signal output. Delay is measured at V_{os} level of +10% from ground (turn-on) or on-state output level (turn-off).

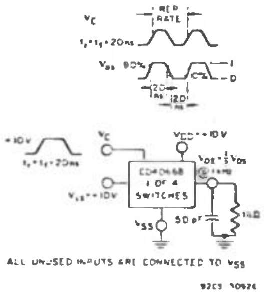


Fig. 15 – Maximum allowable control input repetition rate.

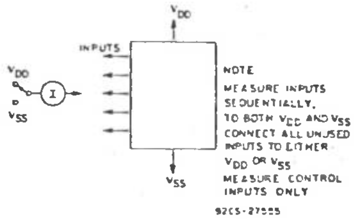

INPUTS
NOTE
MEASURE INPUTS SEQUENTIALLY,
TO BOTH V_{DD} AND V_{SS}
CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}
MEASURE CONTROL INPUTS ONLY
92CS-27555

Fig. 16 – Input leakage current test circuit.

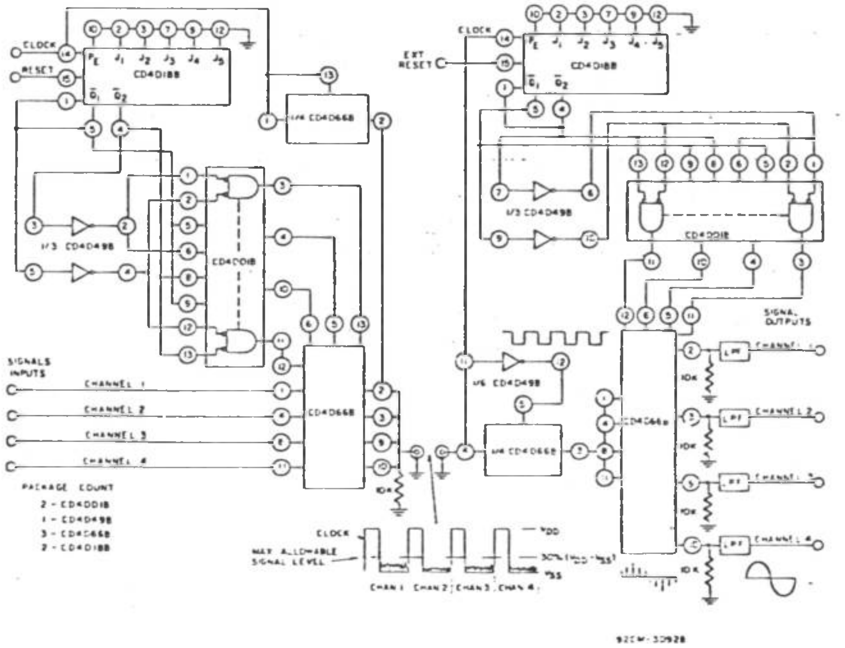


Fig. 17– 4-channel PAM multiplex system diagram.

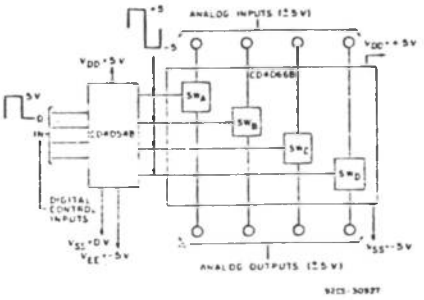
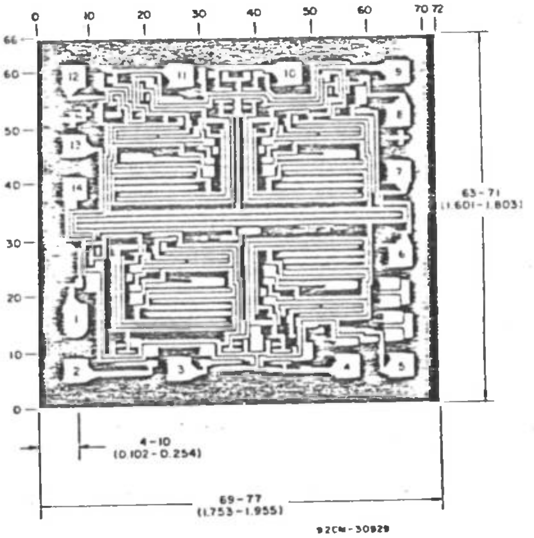


Fig. 18 — Bidirectional signal transmission via digital control logic.



CD4066BH
CHIP PHOTOGRAPH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS 4-Bit D-Type Registers

High-Voltage Types (20-Volt Rating)

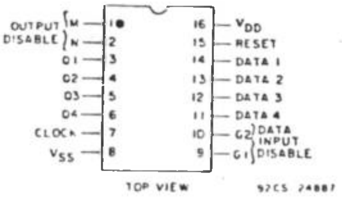
The CD4076B types are four-bit registers consisting of D-type flip-flops that feature three-state outputs. Data Disable inputs are provided to control the entry of data into the flip-flops. When both Data Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Output Disable inputs are also provided. When the Output Disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs are disabled independently of the clock by a high logic level at either Output Disable input, and present a high impedance.

The CD4076B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

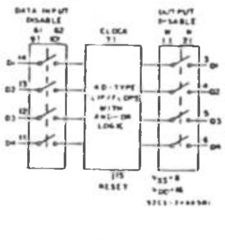
Features:

- Three-state outputs
- Input disabled without gating the clock
- Gated output control lines for enabling or disabling the outputs
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin over full package temperature range:

  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



TERMINAL ASSIGNMENT



FUNCTIONAL DIAGRAM

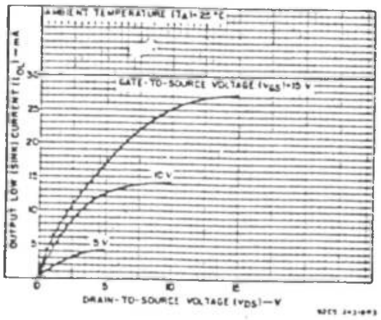


Fig.1 — Typical output low (sink) current characteristics.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5	200	–	ns
	10	80	–	
	15	60	–	
Clock Pulse Width, t_W	5	200	–	ns
	10	100	–	
	15	80	–	
Clock Input Frequency, f_{CL}	5	dc	3	MHz
	10		6	
	15		8	
Clock Input Rise or Fall Time, t_rCL, t_fCL	5	–	15	μs
	10	–	5	
	15	–	5	
Reset Pulse Width, t_W	5	120	–	ns
	10	50	–	
	15	40	–	
Data Input Disable Setup Time, t_S	5	180	–	ns
	10	100	–	
	15	70	–	

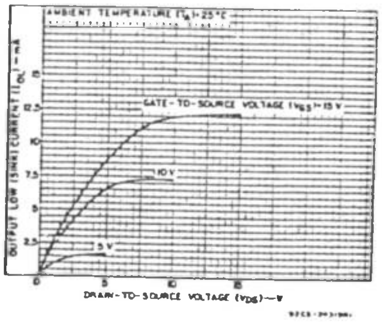


Fig.2 — Minimum output low (sink) current characteristics.

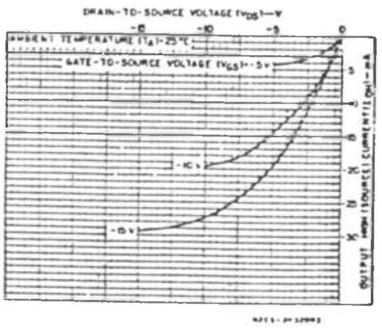


Fig.3 — Typical output high (source) current characteristics.

CD4076B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

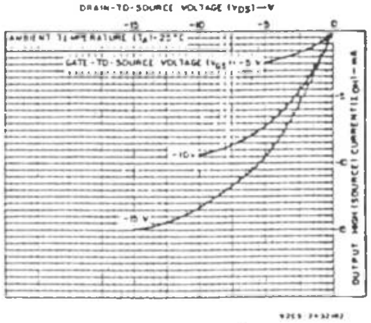
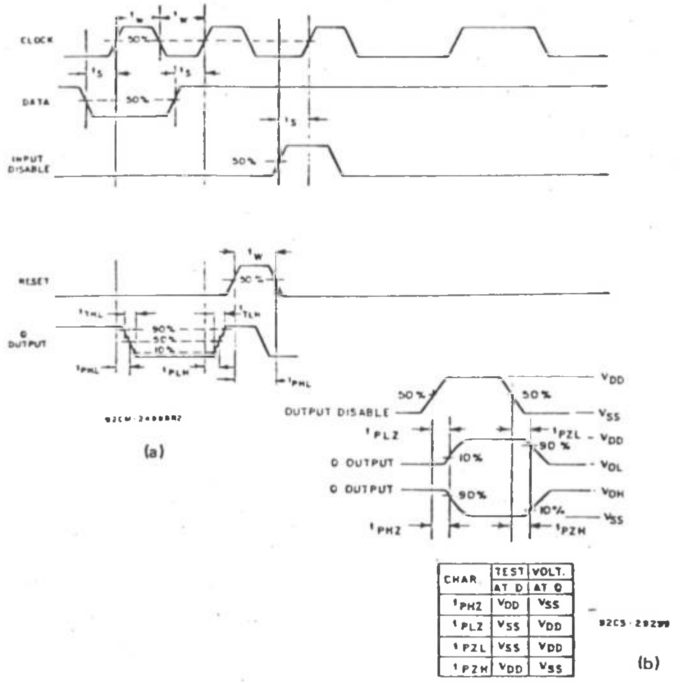


Fig.4 — Minimum output high (source) current characteristics.



CHAR	TEST AT D	VOLT. AT Q
t_{PHZ}	V_{DD}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}
t_{PZL}	V_{SS}	V_{DD}
t_{PZH}	V_{DD}	V_{SS}

Fig.5 — Functional waveforms for CD4076B.

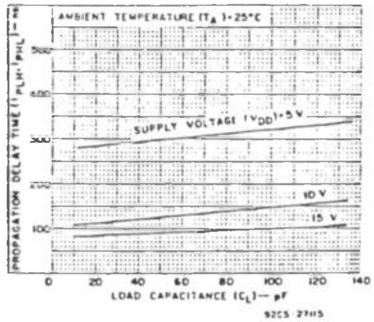


Fig.6 — Typical propagation delay time vs. load capacitance (clock to Q).

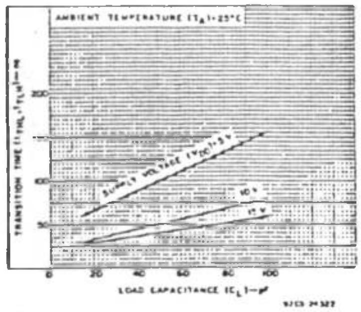


Fig.7 — Typical transition time vs. load capacitance.

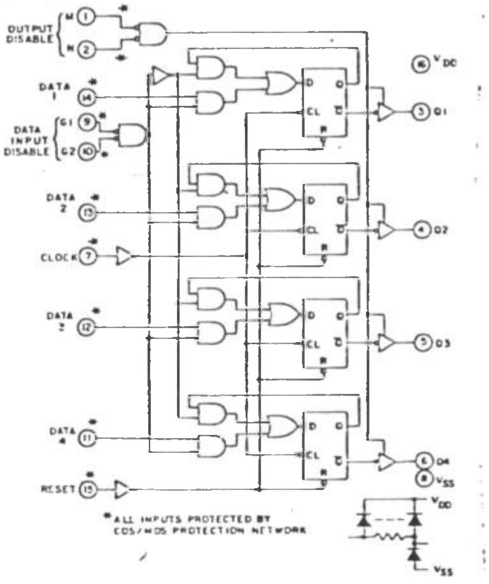
Truth Table

Reset	Clock	Data Input Disable G1	Data Input Disable G2	Data D	Next State Output Q	
1	X	X	X	X	0	
0	0	X	X	X	Q	NC
0	↑	1	X	X	Q	NC
0	↑	X	1	X	Q	NC
0	↑	0	0	1	1	
0	↑	0	0	0	0	
0	1	X	X	X	Q	NC
0	↓	X	X	X	Q	NC

When either Output Disable M or N is high, the outputs are disabled (high impedance state), however sequential operation of the flip flops is not affected.

1 ≡ High Level
0 ≡ Low Level

X = Don't Care
NC = No Change



*ALL INPUTS PROTECTED BY COS/MOS PROTECTION NETWORK

Fig 8 — CD4076B logic diagram.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER-ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (^{o}C) Values at –55, +25, +125 Apply to D, F, H Packages Values at –40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA
3 State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm10^{-4}$	±0.4	μA

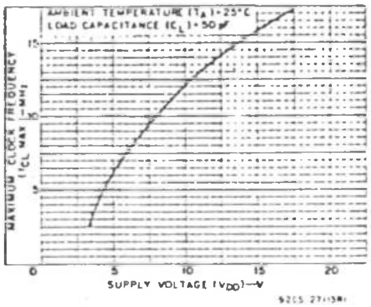


Fig.9 – Typical maximum clock input frequency vs. supply voltage.

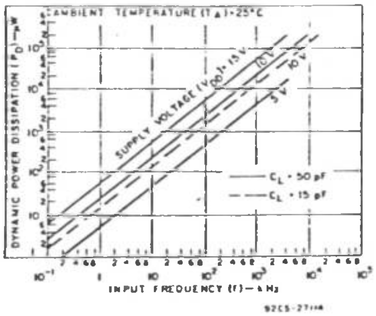
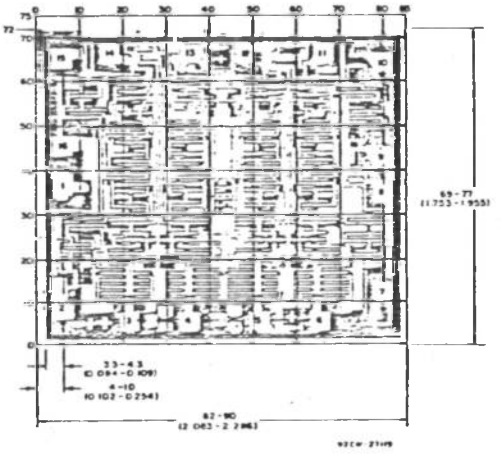


Fig.10 – Typical dynamic power dissipation vs. frequency.



Dimensions and pad layout for CD4076BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$, Input $t_r, t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ (Unless otherwise noted)

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
		V_{DD} V	Min.	Typ.	Max.	
Propagation Delay Time Clock to Q Output, t_{PHL}, t_{PLH}		5	–	300	600	ns
		10		125	250	
		15		90	180	
Reset, t_{PHL}		5		230	460	
	–	10		100	200	
		15	–	75	150	
3-State Output 1 or 0 to High Impedance, t_{PHZ}, t_{PLZ}	$R_L = 1$ kΩ	5		150	300	
		10	–	75	150	
		15		60	120	
3-State High Impedance to 1 or 0 Output, t_{PZH}, t_{PZL}	$R_L = 1$ kΩ	5		150	300	
		10		75	150	
		15		60	120	
Transition Time, t_{THL}, t_{TLH}		5		100	200	ns
		10		50	100	
		15		40	80	
Maximum Clock Input Frequency, f_{CL}		5	3	6	–	MHz
		10	6	12	–	
		15	8	16	–	
Minimum Clock Pulse Width, t_W		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Maximum Clock Input Rise or Fall Time, t_{rcl}, t_{fcl}		5	15	–	–	μs
		10	5	–	–	
		15	5	–	–	
Minimum Reset Pulse With, t_W		5	–	60	120	ns
		10	–	25	50	
		15	–	20	40	
Minimum Data Setup Time, t_S		5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
Minimum Data Input Disable Setup Time, t_S		5	–	90	180	ns
		10	–	50	100	
		15	–	35	70	
Input Capacitance, C_{IN}	Any Input	–	–	5	7.5	pF

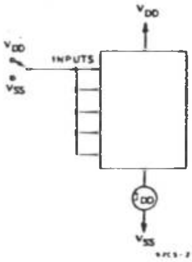


Fig.11 – Quiescent device current test circuit.

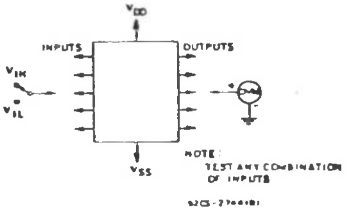


Fig.12 – Input voltage test circuit.

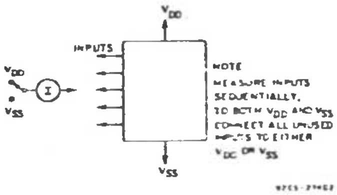

VDD
INPUTS
VDD
I
VSS
NOTE
MEASURE INPUTS SEQUENTIALLY, TO BOTH VDD AND VSS CONNECT ALL UNUSED INPUTS TO EITHER VDD OR VSS
VSS
92CS-27442

Fig. 13 – Input current test circuit.

COS/MOS AND Gates

High-Voltage Types (20-Volt Rating)

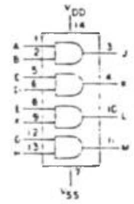
CD4073B Triple 3-Input AND Gate
CD4081B Quad 2-Input AND Gate
CD4082B Dual 4-Input AND Gate

The RCA-CD4073B, CD4081B and CD-4082B AND gates provide the system designer with direct implementation of the AND function and supplement the existing family of COS/MOS gates.

The CD4073B, CD4081B and CD4082B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Features:

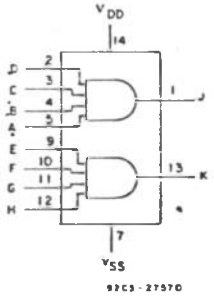
- Medium-Speed Operation – t_{PLH}, t_{PHL} = 60 ns (typ.) at V_{DD} = 10 V
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



CD4081B
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	–0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = –40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	–55 to +125°C
PACKAGE TYPE E	–40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	–65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C



CD4082B
FUNCTIONAL DIAGRAM

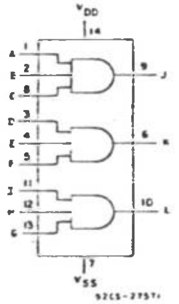
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, Input t_r,t_f=20 ns, and C_L=50 pF, R_L=200 kΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} Volts	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	125	250	ns
		10	60	120	
		15	45	90	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input	–	5	7.5	pF



CD4073B
FUNCTIONAL DIAGRAM

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5	–	5	1.5				–	–	1.5	V
	1	–	10	3				–	–	3	
	1.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

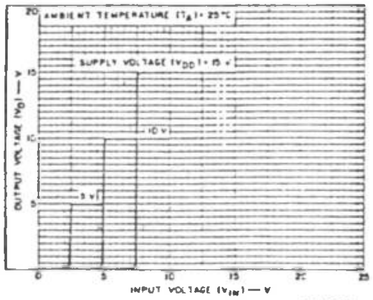


Fig. 3 — Typical voltage transfer characteristics.

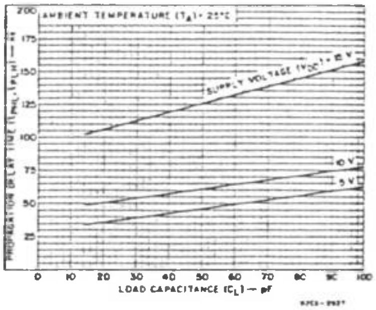


Fig. 4 — Typical propagation delay time as a function of load capacitance.

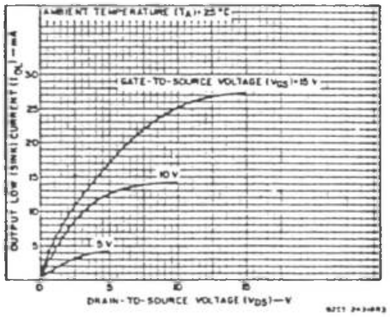


Fig. 5 — Typical output low (sink) current characteristics.

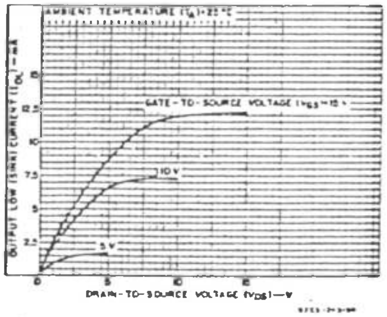


Fig. 6 — Minimum output low (sink) current characteristics.

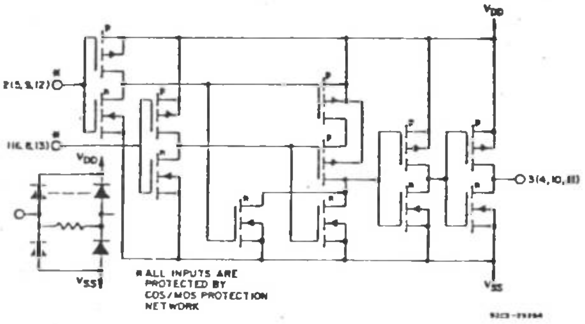


Fig. 1 — Schematic diagram for CD4081B (1 of 4 identical gates).

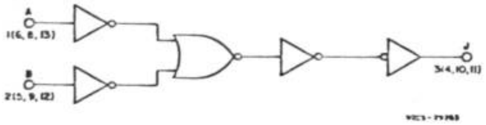


Fig. 2 — Logic diagram for CD4081B (1 of 4 identical gates).

CD4514B, CD4515B Types

COS/MOS 4-Bit Latch/4-to-16 Line Decoders

High-Voltage Types (20-Volt Rating)
CD4514B Output "High" on Select
CD4515B Output "Low" on Select

The RCA-CD4514B and -CD4515B consist of a 4-bit strobed latch and a 4-to-16-line decoder. The latches hold the last input data presented prior to the strobe transition from 1 to 0. Inhibit control allows all outputs to be placed at 0(CD4514B) or 1(CD4515B) regardless of the state of the data or strobe inputs.

The decode truth table indicates all combinations of data inputs and appropriate selected outputs.

These devices are similar to industry types MC14514 and MC14515.

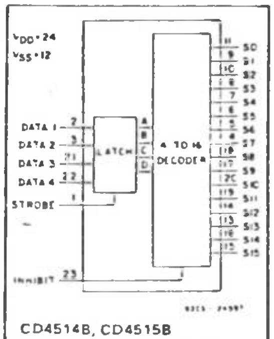
The CD4514B and CD4515B types are supplied in 24-lead hermetic dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in line plastic packages (E suffix), and in chip form (H suffix).

Features:

- Strobed input latch
- Inhibit control
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  - 1 V at V_{DD} = 5 V
  - 2 V at V_{DD} = 10 V
  - 2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Digital multiplexing
- Address decoding
- Hexadecimal/BCD decoding
- Program-counter decoding
- Control decoder



CD4514B, CD4515B
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5 10 15	150 70 40	– – –	ns
Strobe Pulse Width, t_W	5 10 15	250 100 75	– – –	ns

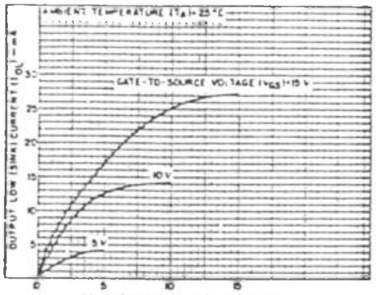


Fig. 1 — Typical output low (sink) current characteristics.

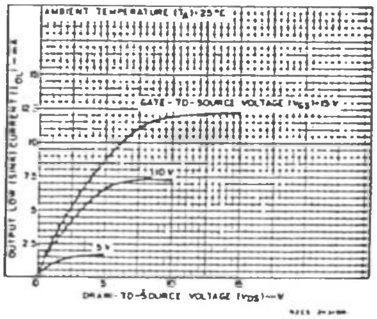


Fig. 2 — Minimum output low (sink) current characteristics.

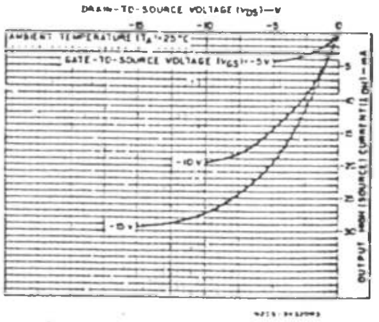


Fig. 3 — Typical output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	µA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	µA

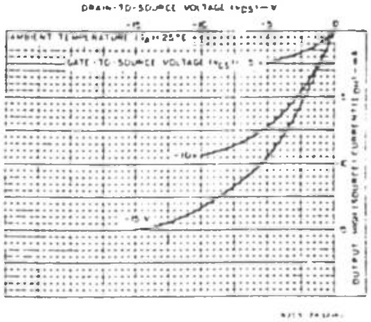


Fig. 4 — Minimum output high (source) current characteristics.

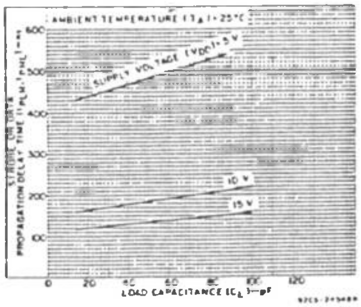


Fig. 5 — Typical strobe or data propagation delay time vs. load capacitance.

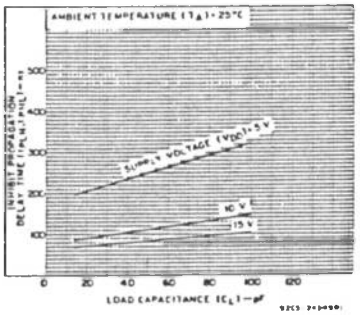


Fig. 6 — Typical inhibit propagation delay time vs. load capacitance.

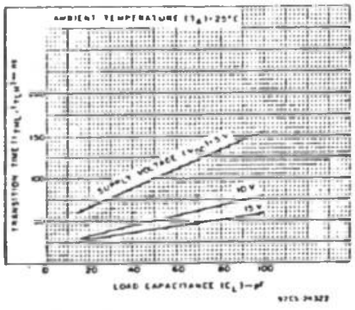


Fig. 7 — Typical low-to-high transition time vs. load capacitance.

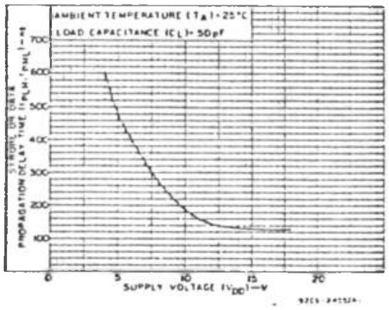


Fig. 8 — Typical strobe or data propagation delay time vs. supply voltage.

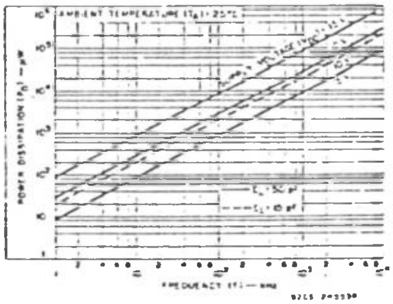


Fig. 9 — Typical power dissipation vs. frequency.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS		UNITS
		V_{DD} V	Typ.	Max.	
Propagation Delay Time: t_{PHL}, t_{PLH} Strobe or Data		5 10 15	485 185 135	970 370 270	ns
Inhibit		5 10 15	250 110 85	500 220 170	
Transition Time, t_{TLH}, t_{THL}		5 10 15	100 50 40	200 100 80	
Minimum Strobe Pulse Width, t_W		5 10 15	125 50 40	250 100 75	ns
Minimum Data Setup Time, t_S		5 10 15	75 35 20	150 70 40	ns
Input Capacitance, C_{IN}	Any Input	—	5	7.5	pF

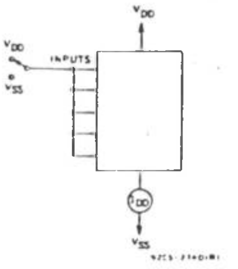


Fig. 10 — Quiescent device current test circuit.

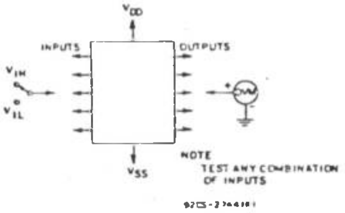
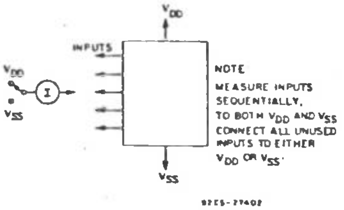


Fig. 11 — Input voltage test circuit.



V_{DD}
INPUTS
V_{DD}
I
V_{SS}
NOTE
MEASURE INPUTS SEQUENTIALLY,
TO BOTH V_{DD} AND V_{SS}
CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}.
V_{SS}
92CS-27402

Fig. 12 — Input current test circuit.

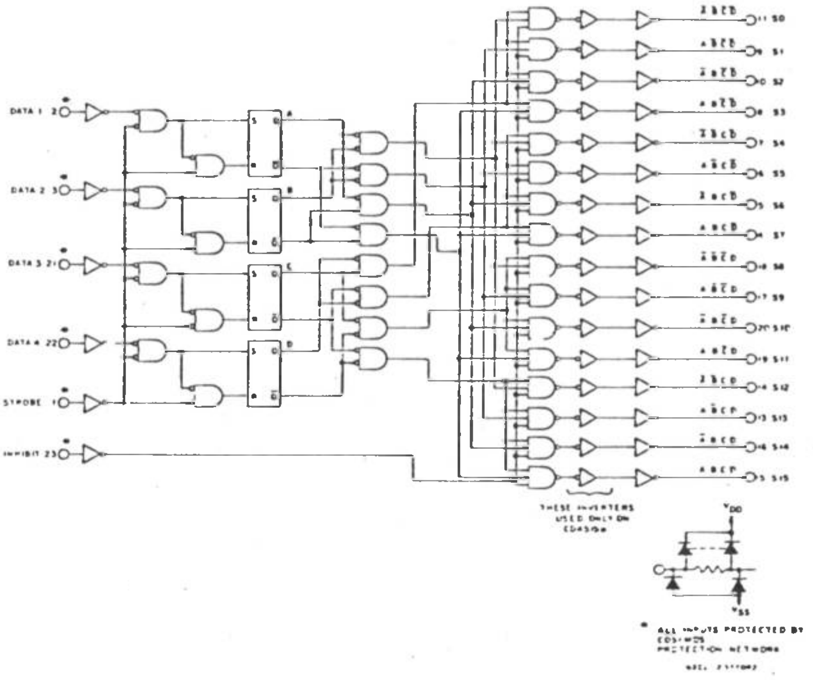


Fig. 13 — Logic diagram for CD4514B and CD4515B.

DECODE TRUTH TABLE (Strobe = 1)

INHIBIT	DECODER INPUTS				SELECTED OUTPUT
	D	C	B	A	CD4514B = Logic 1 (High) CD4515B = Logic 0 (Low)
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, CD4514B All Outputs = 1, CD4515B

X = Don't Care   Logic 1 = high   Logic 0 = low

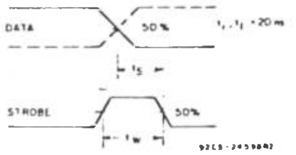
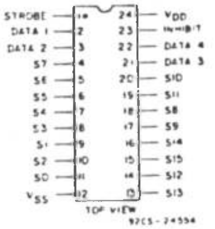
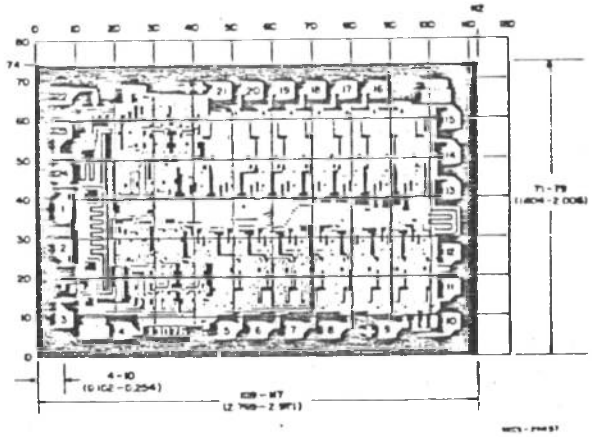


Fig. 14 — Waveforms for setup time and strobe pulse width.



CD4514B
CD4515B

TERMINAL ASSIGNMENT



Dimensions and Pad Layout for CD4515B Chip

(Dimensions and pad layout for the CD4514B are identical)

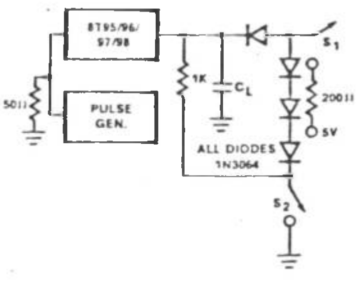
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

DC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	V_{CC} = MIN, I_{IN} = -12mA				
	Input				-1.5	V
	Output to ground				-1.5	V
	Output voltage	V_{CC}= MIN				
V_{OL}		I_{OL} = 48mA			0.5	V
V_{OH}		I_{OH} = 5.2mA	2.4			V
	Input current	V_{CC} = MAX, V_{IN} = 0.5V				
I_{IL}	Low	D_{IS} = 0.5V			-400	μA
		D_{IS} = 2.0V (third state)			-40	μA
I_{IH}	High	V_{IN} = 2.4V			40	μA
I_{OS}	Short circuit output current	V_{CC} = MAX, V_{IN} = 0V, V_{OUT} = 0V	-40	-80	-115	μA

AC TEST CIRCUIT



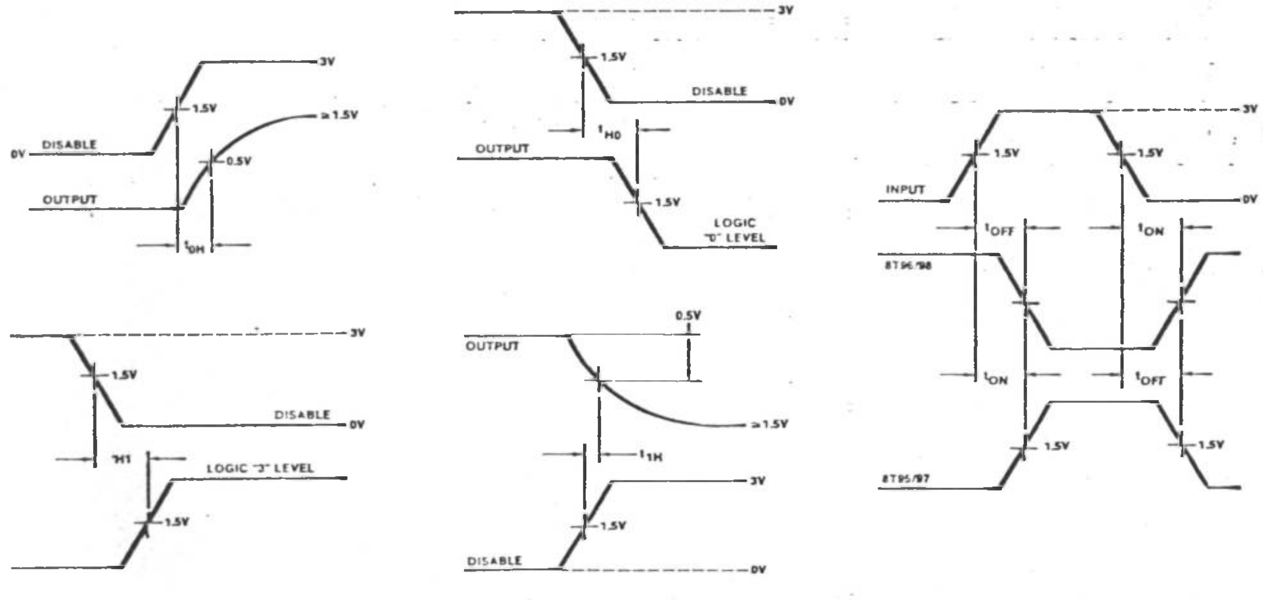
Input Characteristics
PA = 3V, f = 1MHz $t_R = t_F \le 10$ns (10% to 90%)
C_L includes probe and jig capacitance.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TO	FROM	TEST CONDITIONS	8T95/97			8T96/98			UNIT
					Min	Typ	Max	Min	Typ	Max	
	Propagation delay										
t_{ON}		Outputs	Inputs		3	9	13	3	6	10	ns
t_{OFF}		Outputs	Inputs		3	7	12	4	7	11	ns
	Disable to Outputs										
t_{POH}		High Z	Low	S_1, S_2 are closed, C_L = 5pF	3	6	12	5	10	16	ns
t_{PLH}		High Z	High	S_1, S_2 are closed, C_L = 5pF	3	5	10	3	6	10	ns
t_{PHO}		Low	High Z	S_1 is closed, S_2 is open; C_L = 50pF	12	14	25	11	18	24	ns
t_{PHL}		High	High Z	S_1 is open, S_2 is closed; C_L = 50pF	8	19	25	7	15	22	ns

PARAMETER MEASUREMENT INFORMATION

PROPAGATION DELAYS



HIGH SPEED HEX 3-STATE BUFFERS
HIGH SPEED HEX 3-STATE INVERTERS

8T95/8T96
8T97/8T98

8T95-N,F • 8T96-N,F • 8T97-N,F • 8T98-N,F

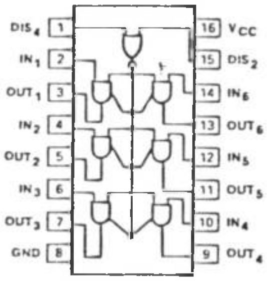
DESCRIPTION

Each of the 3-State Bus Interface Elements described herein has low current PNP inputs and is designed with Schottky TTL technology for ultra high speed. The devices are used to convert TTL/DTL or MOS/CMOS to 3-state TTL Bus levels. For maximum systems flexibility the 8T95 and 8T97 do so without logic inversion, whereas, the 8T96 and 8T98 provide the logical complement of the input. The 8T95 and 8T96 feature a common control line for all six devices, whereas, the 8T97 and 8T98 have control lines for four devices from one input and two from another input.

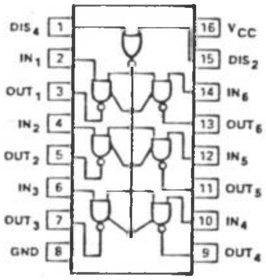
PIN CONFIGURATIONS

N,F PACKAGE

8T95

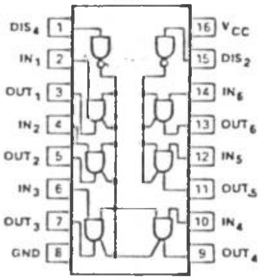


8T96

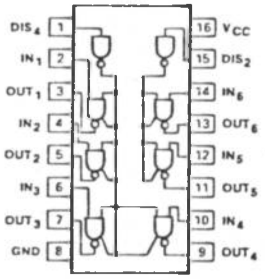


N,F PACKAGE

8T97



8T98

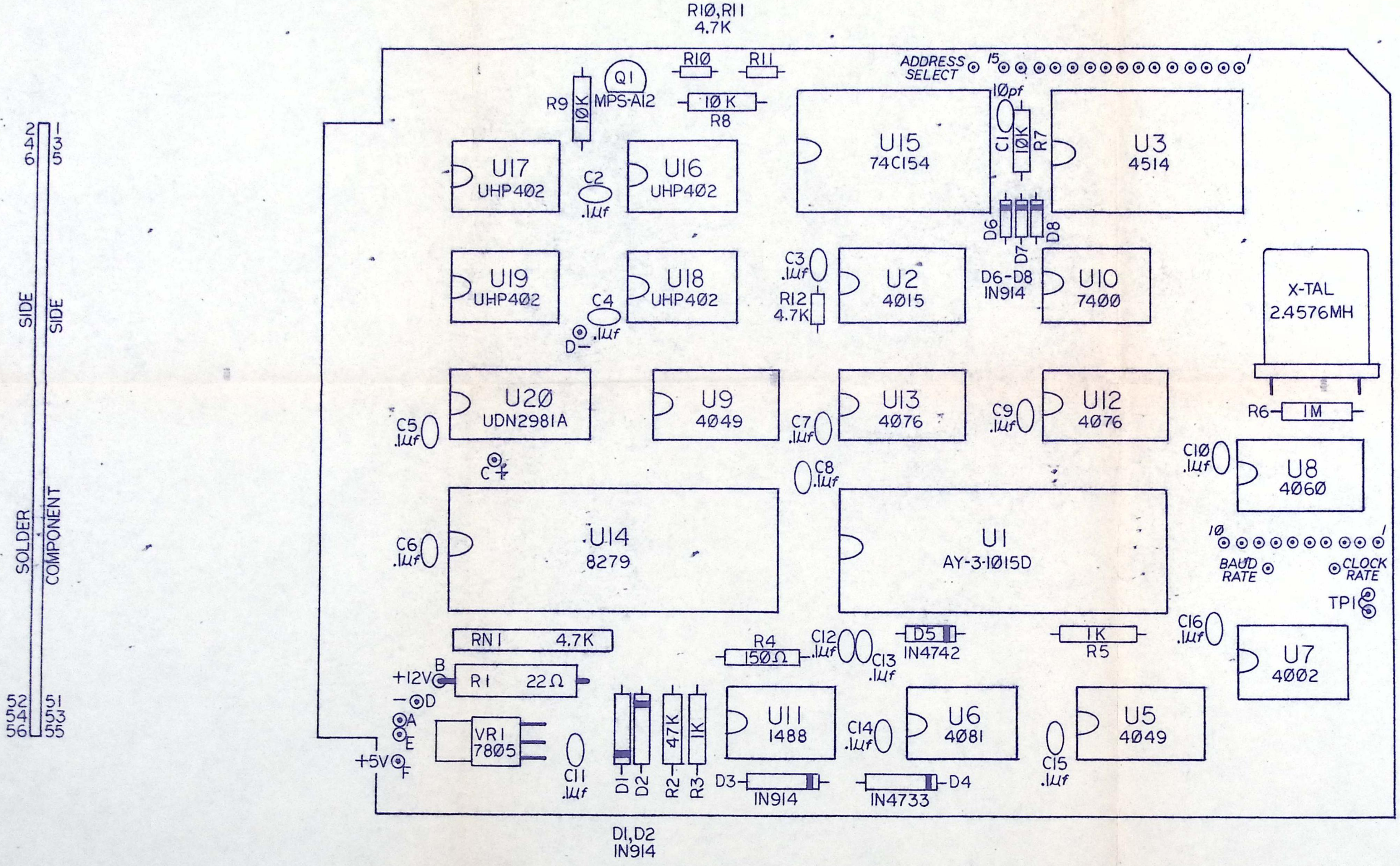


TRUTH TABLE

DEVICE	DISABLE DIS_1	DISABLE DIS_4	INPUT DIS_2	INPUT	OUTPUT
8T95	0	—	0	0	0
	0	—	0	1	1
	0	—		x	H-z
	1	—	0	x	H-z
	1	—	1	x	H-z
8T96	0	—	0	0	1
	0	—	0	1	0
	0	—	1	x	H-z
	1	—	0	x	H-z
	1	—	1	x	H-z
8T97	—	0	0	0	0
	—	0	0	1	1
	—	x	1	x	H-z*
	—	1	x	x	H-z**
8T98	—	0	0	0	1
	—	0	0	1	0
	—	x	1	x	H-z*
	—	1	x	x	H-z**

*Output 5-6 only **Output 1-4 only x = irrelevant

DCN NO	REV	DESCRIPTION	DATE
——	D	REDRAWN	4-23-84



I/O CONTROLS INC.			NEWTOWN, PA.		
TOLERANCES (EXCEPT AS NOTED)	REVISIONS			ASSY, REMOTE SERIAL	
	NO.	DATE	BY		
DECIMAL ±	1			MODEL S-16	
FRACTIONAL ±	2				
	3			DRAWN BY D. HIRTH	SCALE 2X	MATERIAL
ANGULAR ±	4			CHK'D	DATE 4-23-84	DRAWING NO. 200 C4036
	5			TRACED	APP'D	

S-16	C		
200C4036	D		
200 D 1050	E		
DWG NO	REV	REV	REV